Design and Characterization of a 20 Gbit/s Clock Recovery Circuit

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Resumo- **Neste artigo é descrito o projecto e a implementação de uma unidade de recuperação de relógio, para um sistema de transmissão por fibra óptica a 20 Gbit/s. Esta unidade está inserida no demonstrador do projecto "TRAVEL", RACE 2011. A unidade de recuperação de relógio tem uma estrutura em malha aberta baseando-se num filtro de elevado Q com ressonador dieléctrico.**

Apresenta-se a caracterização eléctrica desta unidade e a sua sensibilidade à dessintonia. Os resultados experimentais mostram que este tipo unidade é um solução bastante atractiva para os sistemas ópticos a muito alto ritmo de transmissão englobados na futura norma STM-128.

Abstract- **In this communication we report the design of a clock recovery circuit produced for the 20 Gbit/s demonstrator of the RACE 2011 project "TRAVEL" of the European Community. The clock recovery circuit is based on an open loop structure using a dielectric resonator narrow bandpass filter with high Q.**

A detailed electrical characterization of the circuit and also its sensitivity to temperature and detuning variations are presented. The experimental results show that the circuit is a very attractive solution for the forthcoming STM-128 optical links.

I. INTRODUCTION

For very high transmission rates, the clock recovery circuit (CRC) is the one of the most critical receiver units. It is essential for any retimed receiver to have a high quality CRC to provide from the received data signal, a very precise local clock in order to perform accurately the regeneration and demultiplexing operations.

Clock recovery circuits can be classified into two groups: open-loop structures and closed loop or adaptive structures. The former is usually built using a nonlinearity which is necessary whenever the incoming signal lacks a discrete spectral line at the transmission rate and a narrowband filter to take out this spectral line from the remain spectrum. The latter approach makes use of the phase-lock principle and it may simply consist of a nonlinearity followed by a PLL or it can take more complex forms such as maximum-likelihood trackers [1] or early late gate bit synchronizers [2]. From a conceptual point of view the adaptive approach is preferable since the phase-lock principle has inherent AFC capabilities and thus one can offer low bandwidths without loosing tuning capabilities. Also this approach offers the potential of complete integration. However for the highest bit rates pursued at the moment the technology needed for a good design is still not completely mature and the open loop solution based on a high Q filter is preferable.

In this communication we report the design and characterization of a clock recovery circuit based on this second solution incorporated into 20 Gbit/s demonstrator of the RACE 2011 project "TRAVEL" ("(HD) TV Transport on Very High Bitrate Optical Links"). Table 1 summarises the required electrical specifications.

TABLE 1
ELECTRICAL SPECIFICATIONS OF THE CLOCK RECOVERY CIRCUIT

Operating Frequency	F1=19.90656 Gbit/s (2*STM-64)
Data Input	250 mVpp/side, 50Ω to ground
Clock Output	250 mVpp/side, 50Ω to ground
Dynamic Jitter clock output	< 0.025 UI (RMS)
Static Jitter clock output	< 0.1 UI
Operating Temperature	+10 to 50 (°C)

II. CIRCUIT DESIGN

The implemented CRC based on open-loop structure is illustrated by the block diagram depict in Fig. 1. The circuit includes a pre-amplifier, a pre-filter, a nonlinear circuit (NLC), a dielectric resonator (DR) filter and a narrow bandwidth amplifier.

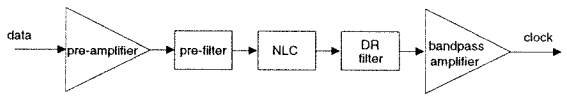


Fig. 1 Simplified block diagram of a clock recovery circuit based on open loop structure.

The pre-amplifier has the main purpose of providing a suitable level to drive the non-linear circuit. The pre-filter is intended to shape the signal so that the jitter caused by the pattern fluctuations is reduced [3]. This filter consists of a microstrip coupled line section centred at 15 GHz. The overall transfer function of the pre-amplifier more pre-filter when combined with input data signal of raised-cosine formatting with approximately 50% roll-off gives a

significant reduction of the jitter caused by the data fluctuations.

The non-linearity (NL) was built using a GaAs FET device biased in the subthreshold region in such a way that half the signal excursion fall below the pinchoff voltage, providing a nonlinearity close to a truncated square law device. For the bit rate under consideration the solution of using an unbalanced NL was chosen instead of the balanced NLs. The unbalanced NLs are simpler to implement and robust enough to be used in a wide class of practical systems at multigigabit regime [4]. It was demonstrated from simulation study [5] that for raised cosine elementary pulses with moderate to high roll-off factors the degradation in performance by using this type of truncated NL is negligible compared with the more common absolute value and full squarer NLs.

The performance of the CRC is highly dependent on the narrow band filter efficiency in filtering the clock line from the continuos spectrum. This filter must have a very high quality factor, a precise center frequency with a low temperature drift. Fig. 2 shows the range of frequencies where different technologies used to build the narrow band filter.

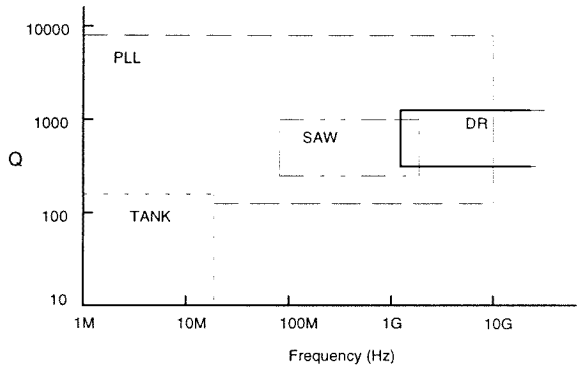


Fig. 2 Different technologies used to build the narrow band filter as a function of the clock rate

At low bit rates the narrowband filter is usually a tuned LC network. Up to a couple of Gbit/s, filters that exploit the interference of acoustic surface waves (SAW) have been used [6]. However for bit rates above a couple of Gbit/s, SAW filters become very difficult to manufacture, because the required spacing between electrodes is very small. For these frequencies the most useful device to build the passive filter is the DR filter. Considerable progress has been done in the last years towards providing DR with good stability in temperature and losses considerably inferior to the ones obtained with SAW devices. These features make the DRs a good choice for the bit rates in the range 5-20 Gbit/s [7-9]. Furthermore due to the high dielectric constant, the devices are available for these frequencies in small sizes which enables circuit miniaturisation. Table 2 summarises the electrical and physical characteristics of the commercial DRs suitable to implement the high Q filter for 20 Gbit/s CRCs [10-11].

TABLE 2
DRS CHARACTERISTICS APPLIED IN FILTER PROTOTYPES

Manufacturer	Siemens	Murata
Reference	B69-500-C2008	DRD033EC015
Dielectric Constant (ε_r)	29	24.5
Q_u at 20 GHz (=1/tangδ)	4200	10000
Shape	cylindrical	cylindrical
Diameter (mm)	3.1	3.33
Thickness (mm)	1.2	1.48
Temp. Coefficient (ppm/°C)	0	0
Available Temp. Coefficients (ppm/°C)	-3; 0; 3; 6; 9; 12	0; 2; 4; 6

The Q of the DR filter represents a trade-off between two factors: the allowable dynamic jitter and the sensitivity to detuning. In order to minimise the dynamic jitter the Q value should be the highest possible. However due to ageing and temperature effects the filter may undergo some detuning. The detuning affects the performance in two ways:

- It will cause a static phase offset of the recovered clock which shifts the average sampling point from its optimum position and causes a performance degradation.
- It will give rise to an increase of the dynamic jitter. With the DR detuned the amplitude of the filtered discrete spectral line is reduced thus enhancing the relative power of the noise sidebands. The increase in jitter is still more pronounced than the inverse of the discrete line reduction for the following reason: the disturbance at the input of the filter is a nonstationary process and its in-phase component is stronger than the quadrature component [12]. If the DR is perfectly tuned only the quadrature component causes phase jitter, the in-phase component causes only amplitude fluctuations. With detuning, part of the AM noise will be converted into FM noise thus increasing the jitter. For robustness against detuning, the value of Q should be low.

Assuming a maximum detuning of ±0.5/1000 and taking the targets of 0.025UI rms for the dynamic jitter and 0.1 UI maximum static offset, it was found following an approaching similar to Gameiro [13] that the optimum Q for the DR should be near 700.

Several filter versions have been tested and implemented using DRs whose characteristics are illustrated in Table 2. The DRs were polished to decrease slightly the thickness with the intend that the resonant frequency was in the range -10% to -5% of resonant frequency. The final frequency tuning was accomplished by a metallic tuning screw. Using these procedures the DRs can be tuned for the desired resonant frequencies without significant degradation of the Q-factor and also good temperature stability.

Table 3 summarises the experimental maximum variation range of the insertion loss and phase slope for a Q_L-factor in range 600 to 800.

TABLE 3
ELECTRICAL CHARACTERISTICS OF DR-FILTERS FOR A Q-FACTOR IN RANGE OF 600 TO 800

Q-factor	600 to 800
Phase slope	3°/MHz to 4°/MHz
Insertion loss at center frequency	<4.5 dB (with conectores)

The experimental magnitude and phase responses of the DR filter are illustrated in Fig. 3. The insertion loss, including the SMA connectors, is 2.7 dB, the Q value is approximately 750 and the phase slope is 4.4°/MHz.

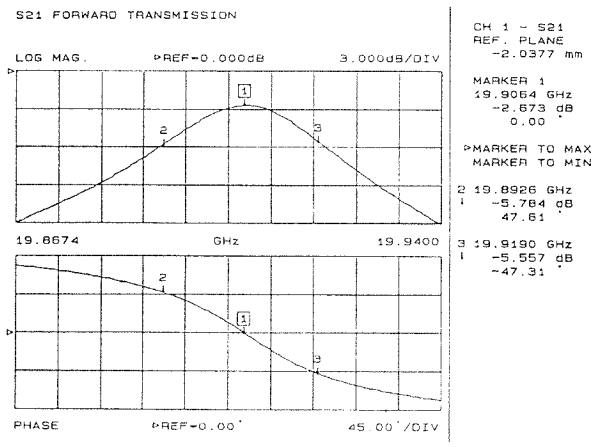


Fig. 3 - The experimental magnitude and phase responses of the dielectric resonator filter

Fig. 4 shows the resonance frequency drift of the filter when a DR with a temperature coefficient of 0ppm/°C was used. From the experimental data the temperature coefficient of DR filter is -4ppm/°C (-80KHz/°C). This temperature dependence can be compensated by using a DR with a symmetric temperature coefficient. Such DRs are commercially available, for example from Murata DRD033EE015 [10]. However this has not been done since for the whole temperature operation (+10 to 50°C) the static jitter at the clock output is less than the project specifications shown in Table 1 as will be illustrated by the experimental results presented in next section.

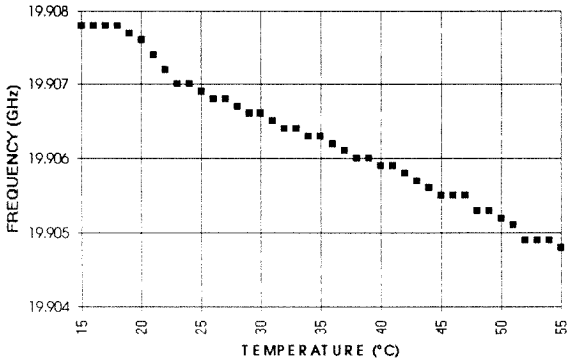


Fig. 4 - Temperature behaviour of DR filter

Figure 5 shows the produced 20 Gbit/s DR filter prototypes with and without the cover case. The physical sizes of these units are 19.5×35.1×18 mm (L×W×H) and use SMA connectors.

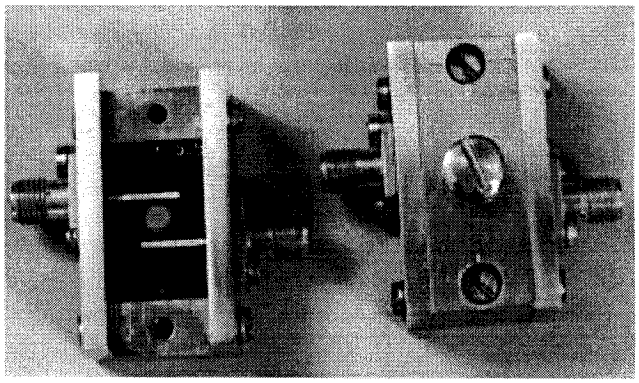


Fig. 5 - 20 Gbit/s DR filter prototypes with and without the cover case.

The clock amplification stage has three main purposes: To provide the required clock signal levels, to reduce the magnitude of the DR filter spurious modes and also to isolate the clock recovery circuit system from the subsequent units. This amplifier stage consists of two cascaded Ka-band pseudomorphic HJ FET chip transistors (NEC-NE32400) assembled on a hybrid form. Microstrip coupled lines instead of chip capacitors were used for DC decoupling. Using this approach a symmetric narrow bandwidth with a high roll-off attenuation out-of-band were achieved as illustrated from the measured S parameters depict in Fig. 6. The pass-band gain is approximately 12.7 dB.

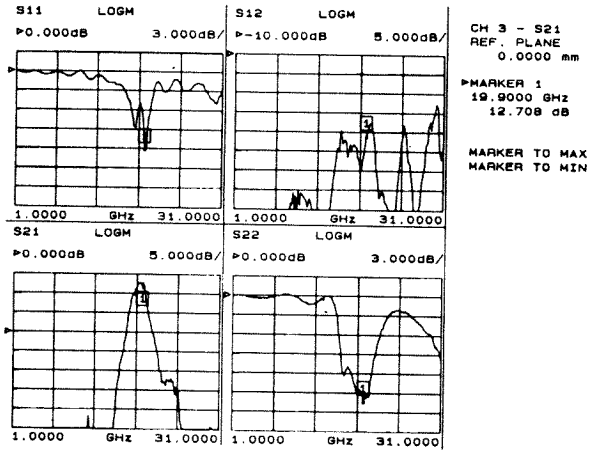
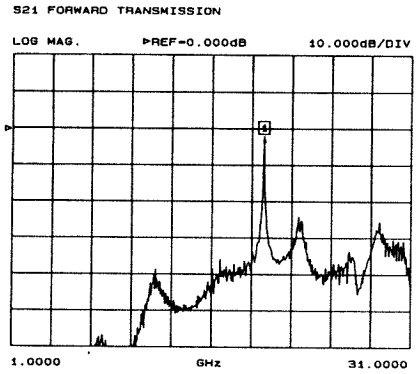


Fig. 6 - Frequency characterization of clock amplification stage

The advantages of using bandwidth amplifier as active filter is better illustrated in Fig. 7 showing the frequency responses of the DR filter and DR filter + Amplifier. From these figures it can be concluded that the out-of-band insertion loss was significantly increased by using this amplifier stage.

a)



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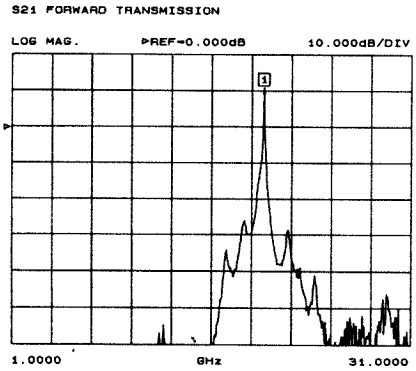


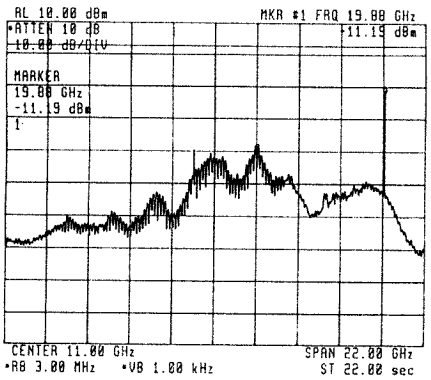
Fig. 7- Frequency response of DR filter without bandpass amplifier (a) and with bandpass amplifier (b).

III. EXPERIMENTAL RESULTS OF OVERALL CIRCUIT

Due to the lack of commercial data pattern generators for the bit rates under consideration, the 20 Gbit/s signal was generated using a 10 Gbit/s pseudo-random bit sequence (PRBS), which was split into two sequences and one of them delayed. After that the two sequences were multiplexed giving the 20 Gbit/s signal. Using this setup, we obtained the spectral and time domain measurements of the clock recovery circuit, for two multiplexed 2^{23}-1 NRZ pseudo-random bit sequences (PRBS), illustrated in Figs. 8 and 9.

Fig. 8a shows the signal spectrum at the nonlinearity output, clearly showing a well-defined discrete line at the bit rate, while Fig. 8b illustrates the spectrum at the CRC output showing a recovered clock line with a power of approximately -2 dBm on 50Ω.

a)



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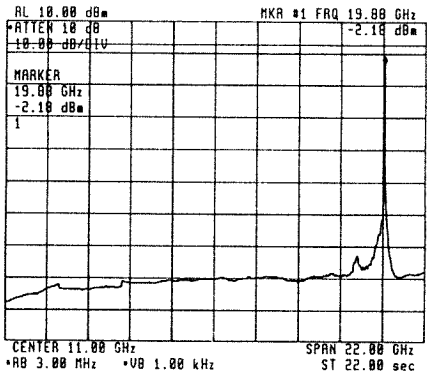

Fig. 8 - Signal spectra at nonlinearity output (a) and at clock recovery unit output (b)

Fig. 9 shows the eye diagram of the input waveform and the recovered clock with an amplitude of approximately 500 mVpp.

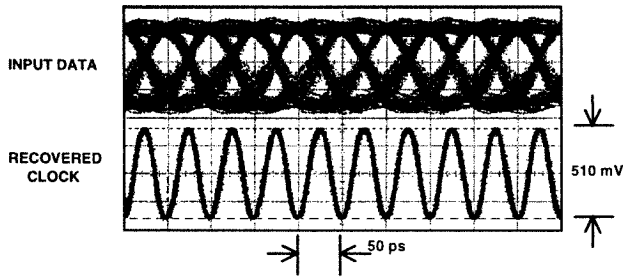

Fig. 9- Time domain waveforms

The jitter performance of the CRC for the PRBS of lengths 2^7-1 and 2^{23}-1 is shown in Figs. 10 where the measured RMS dynamic jitter is plotted for various values of the filter detuning. For a PRBS of length 2^{23}-1 it can be seen that specifications for a maximum dynamic jitter of 0.025 UI allows a detuning larger than ±10MHz. Clock phase deviation versus filter detuning is illustrated in Fig. 11. For a maximum phase deviation (static jitter) of 0.1 UI the CRU allows a detuning of ±6MHz. As refereed in previous section, the measured temperature sensitivity of the DR filter was -4 ppm/°C (-80KHz/°C) and consequently the allowable detuning range of ± 6 MHz accommodates a temperature span higher than the operating temperature specifications of 10°C to 50°C.

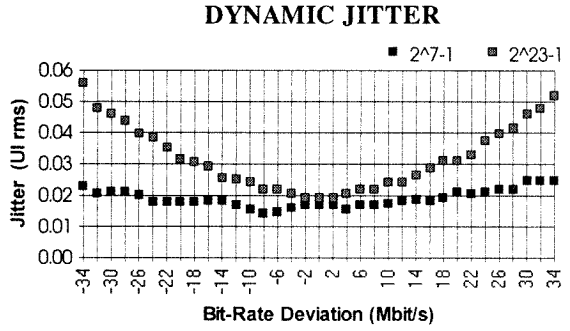

Fig. 10 - Rms dynamic jitter versus bit-rate deviation for the PRBS of 2^7-1 and 2^{23}-1

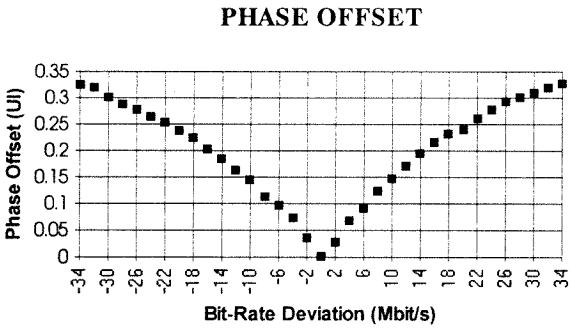

Fig. 11 - Clock phase deviation as a function of bit-rate deviation (filter detuning).

Fig. 12 illustrates the clock amplitude versus filter detuning. For an allowable detuning of ± 6 MHz the clock amplitude varies between 480 mVpp and 510 mVpp that represents only 6% of variation.

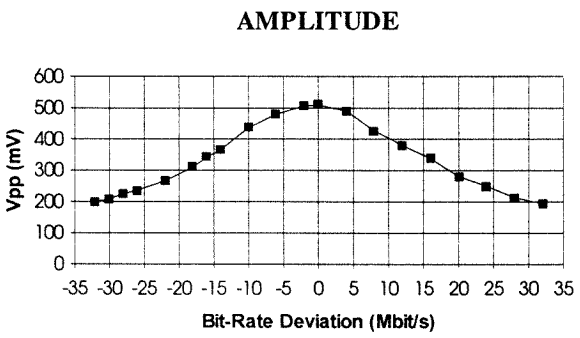

Fig. 12- Clock amplitude versus bit-rate deviation (filter detuning).

IV. CONCLUSIONS

A clock recovery circuit for an optical fiber communication system at 20 Gbit/s was build and characterized. This unit uses a dielectric resonator to implement a high Q filter, a pre-filter to reduce data pattern jitter and also a bandpass amplifier with sharp cut-off to reduce the DR spurious resonances and noise. Particular emphasis has been put on the design of the circuit to guarantee easy reproducibility, manufacturing and good performance over a wide range of operating conditions to make the circuit suitable for practical systems.

As a main conclusion, it turns out that the approach followed provides an economic and robust solution for practical implementation of the very high speed bit rate receivers for the forthcoming SDH hierarchies.

V. ACKNOWLEDGEMENTS

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