Delay Analysis of a Current Source CMOS Inverter for use in Voltage Controlled Delay Lines

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Resumo - **Este artigo apresenta um elemento de atraso CMOS com aplicação em linhas de atraso controladas por tensão, como é o caso das utilizadas nas *Delay Locked Loops*. Este elemento baseia-se num inversor modificado com fonte de corrente. A análise feita mostra uma maior linearidade da sua característica de atraso versus tensão de controlo do que a obtida através de células de atraso convencionais. São derivadas expressões para o tempo de atraso da célula proposta em termos dos parâmetros físicos dos seus componentes e apresentados resultados comparativos destas expressões com simulações feitas em SPICE.**

Abstract - **An analysis is performed on the operation of a modified current-source loaded inverter, showing that the proposed modification leads to a more linear characteristic, in terms of delay versus control voltage, than the one obtained with traditional current-starved inverters. A delay cell designed around this inverter is presented. The proposed circuit is intended to be used as a delay element in a delay chain, such as those used in Delay Locked Loops. Expressions are derived for the time delay of the cell in function of physical parameters. Results of a comparison between the analytically derived delays and the delays obtained from SPICE simulation are presented.**

I. INTRODUCTION

Voltage controlled delay elements play an important role in interpolating time functions inside clock cycles. An example is the delay chain based Delay Locked Loops (DLLs) where the delay elements are continuously adjusted to a time reference. Current starved (current shrinking) inverters are the most usual delay elements used in voltage controlled delay chains [1-4]. This simple configuration has a very non-linear delay characteristic, even if improved current mirror circuits are used [5]. Applications based on delay elements where the gain is dependent on the point of lock, like DLLs, seems to have more constant dynamic behavior if more linear delay elements are used. The delay element designed around an inverter loaded with a current source and an additional static inverter, performing buffering and signal reshaping, shows smaller differential non-linearity values, and thus it is more suitable for these applications.

Since analytical expressions are more useful in understanding the behavior of circuits because they give insight into the dependence on physical parameters, a simple analytical expression for the delay of a inverter with a current source is derived in Section II. In Section III results are extended to find the overall delay of the proposed element. In section IV an example shows the validation of results by a comparison with SPICE results. Section V is dedicated to conclusions.

II. ANALYSIS

A. MOSFET Model and Delay Element

In this paper, all analysis is based on the Shockley MOSFET model. This simple square-law, long-channel transistor model is widely used in treating MOSFET circuits since more advanced short-channel models cannot be easily handled analytically [6]. For short-channel MOSFETs this model cannot reproduce the voltage-current characteristics mainly because it does not include the velocity saturation effects of carriers [7]. However, results based on this simple model are sufficient accurate for conservative CMOS technology. When deviations like short-channel effects must be taken into account, empirical corrections are possible based on insight gained from results obtained from this model [6].

In the Shockley model, the drain current I_D is given by:

$$I_D = \begin{cases} 0 & (V_{GS} \le V_{TH}) \\ K\left[(V_{GS} - V_{TH})V_{DS} - 0.5{V_{DS}}^2\right] & (V_{DS} < V_{DSAT}) \\ 0.5K\left(V_{GS} - V_{TH}\right)^2 & (V_{DS} \ge V_{DSAT}) \end{cases} \quad (1)$$

where V_{DSAT} ($=V_{GS}$-V_{TH}) is the drain saturation voltage, V_{TH} is the threshold voltage and K is the transistor gain parameter.

Figure 1 shows the non-inverting delay element consisting of an inverter with a current source load and an additional static inverter. The delay of the falling edge is controlled by a current imposed by means of a control voltage V_C. Inverters with current sources allow higher values of charging currents which permits the inclusion of a capacitor C as shown on Fig. 1. The effect of the last inverter is only considered in Section III because C can be made large enough to neglect parasitics. The delay is then determined by the current control voltage V_C and capacitor C rather then relying on parasitics.

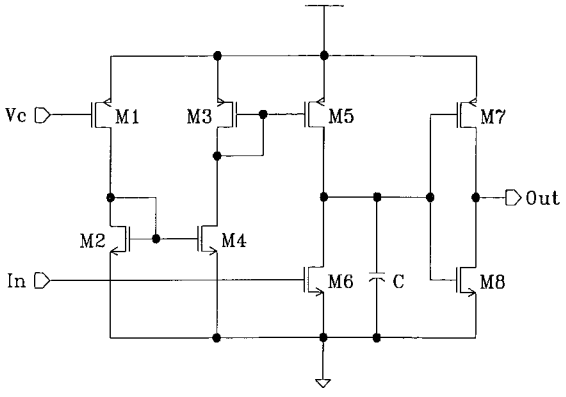

Fig. 1 - Schematic of the delay element.

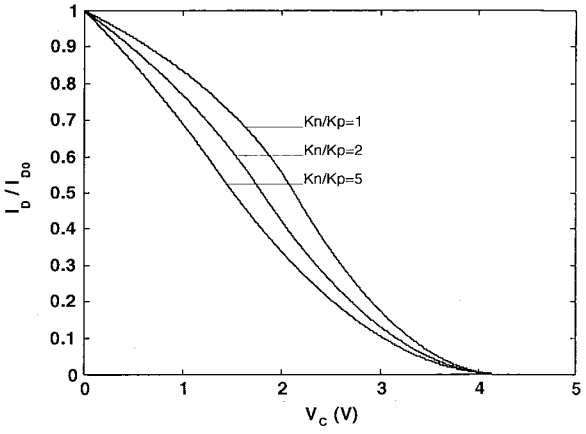

Fig. 2 - Normalized current as a function of V_C.

B. Capacitor Charging Current

The capacitor charging current is determined by the control voltage V_C, sizing of transistors M1 and M2 and current gain A_I of the current mirrors M2-M4 and M3-M5.

The current I_D on transistors M1 and M2 could be calculated by means of (1), considering the appropriate transistor operating regions (assuming that $V_C<V_{DD}-V_{TP}$[1], *i.e*, transistors M1 and M2 are conducting). M2 is diode connected and thus always in saturation, so two regions can be defined, corresponding to the PMOS transistor being in the linear and in the saturation regions. From the linear condition for a PMOS transistor $V_{DSP}<V_{GSP}-V_{TP}$ and taking into account that $V_{DSP}=V_{DD}-V_{GSN}$, $V_{GSP}=V_{DD}-V_C$ and $V_{GSN}=V_{TN}+\sqrt{2I_D/K_N}$, the PMOS transistor is in the linear region (region 1) if:

$$I_D > \frac{K_N}{2}\left(V_C+V_{TP}-V_{TN}\right)^2 \tag{2}$$

and in the saturation region (region 2) if:

$$I_D < \frac{K_N}{2}\left(V_C+V_{TP}-V_{TN}\right)^2 \tag{3}$$

The current I_D as a function of V_C in the two regions can now be calculated (assuming that $V_{TN}=V_{TP}=V_T$).

Region 1 (linear): In this region the PMOS transistor is in the linear region and current I_D is given by:

$$I_D = K_P\left[\left(V_{GSP}-V_T\right)V_{DSP}-0.5{V_{DSP}}^2\right] \tag{4}$$

Substituting the corresponding values for V_{GSP} and V_{DSP} and solving for I_D, we obtain:

$$I_D = \frac{K_N}{2}\left(\frac{K_P}{K_N+K_P}\right)^2 \cdot\left[V_C+\sqrt{{V_C}^2+\frac{K_N+K_P}{K_P}\left(V_{DD}-V_T\right)\left(V_{DD}-V_T-2V_C\right)}\right]^2 \tag{5}$$

Region 2 (saturation): In this region the PMOS transistor is also saturated and the current is simply:

$$I_D = \frac{K_P}{2}\left(V_{DD}-V_T-V_C\right)^2 \tag{6}$$

Figure 2 shows the normalized current as a function of V_C, according to (5) and (6), for different values of K_N/K_P. We can see that for values of $K_N / K_P \geq 5$ and for values of V_C in the range 0-2V a normalized current is approximately a linear function of V_C. The current can thus be written as:

$$I_D = I_{D0}.\left(1-mV_C\right) \tag{7}$$

where I_{D0} is obtained from (5) for $V_C=0$ and equals:

$$I_{D0} = \frac{K_N K_P}{2\left(K_N+K_P\right)}\left(V_{DD}-V_T\right)^2 \tag{8}$$

To calculate m one needs another point on the curve. To minimize the error for all values of K_N/K_P, we consider the second point to be at the intersection of the I_D curve with the curve that delimits the two regions of the PMOS transistor as indicated by (2). Solving for equal values of I_D, we obtain the corresponding point (V_{CSAT}, I_{DSAT}/I_{D0}):

$$V_{CSAT} = \frac{V_{DD}-V_T}{1+\sqrt{\frac{K_N}{K_P}}} \tag{9}$$

and:

[1] $V_{TP}=|V_{GSP}|$. Throughout this paper all PMOS transistors operating values are absolute.

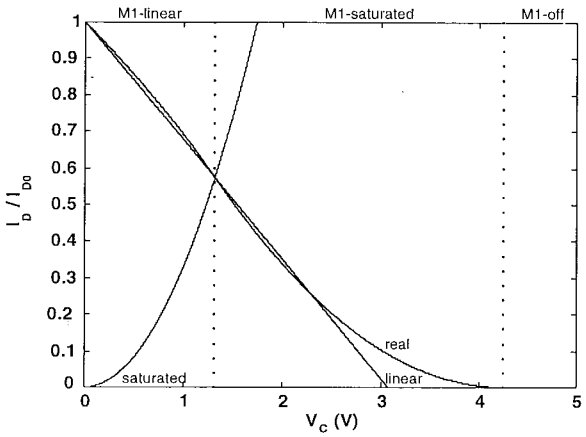

Fig. 3 - Normalized real, saturated and linear curves of current.

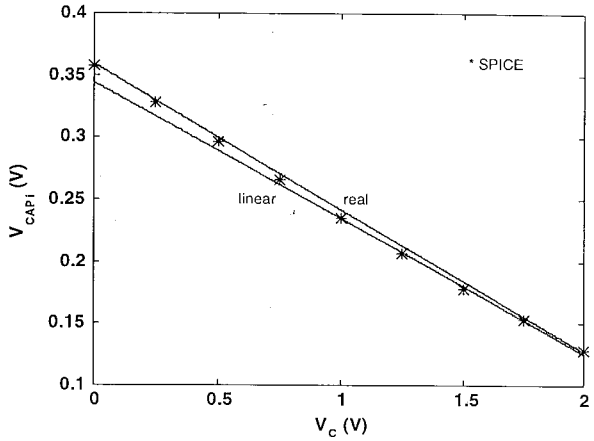

Fig. 4 - Initial capacitor voltage from eq. (13) (real), eq. (14) (linear) and from SPICE with values of Section IV.

$$I_{DSAT} = \frac{K_N + K_P}{K_P\left(1+\sqrt{\frac{K_N}{K_P}}\right)^2} I_{D0} \qquad (10)$$

Substituting (9) and (10) in (7), we obtain:

$$m = \frac{\left(1+\sqrt{\frac{K_N}{K_P}}\right)^2 - \left(1+\frac{K_N}{K_P}\right)}{(V_{DD}-V_T)\left(1+\sqrt{\frac{K_N}{K_P}}\right)} \qquad (11)$$

Figure 3 shows normalized real, saturated and linear curves of current for $K_N/K_P=5$.

The capacitor charging current (the current through M5) is modeled simply as the multiplying of the current I_D by the current gain of the current mirrors (A_I):

$$I_C = A_I I_{D0}(1 - mV_C) \qquad (12)$$

C. The Delay Equation

To calculate the delay of the current source inverter one must calculate the initial capacitor voltage (V_{CAPi}) first. In order to do this, as the delay is calculated in the falling edge, the gate of M6 is assumed to be at V_{DD} (input signal at high level) and the capacitor voltage constant and equal to its minimum value. In this condition the current in M6 equals the current in M5 with M6 in linear region. Equating the corresponding values of current we find that the initial capacitor voltage (equal to the V_{DS} of M6) is given by:

$$V_{CAPi} = (V_{DD}-V_T)\left[1-\sqrt{1-\frac{A_I K_N K_P}{K_N'(K_N+K_P)}(1-mV_C)}\right] \qquad (13)$$

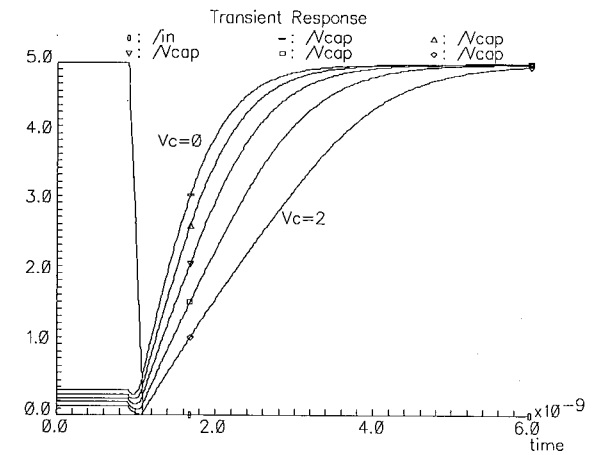

Fig. 5 - Simulated output capacitor voltage as function of V_C.

where K_N' is the gain of transistor M6. This equation can be simplified using the series expansion of the square-root, giving:

$$V_{CAPi} = \frac{1}{2}(V_{DD}-V_T)\frac{A_I K_N K_P}{K_N'(K_N+K_P)}(1-mV_C) \qquad (14)$$

provided that the subtracting term under the square-root is much smaller than one. This is a good approximation as we can see in Fig. 4. The errors in initial capacitor voltage are larger for small values of V_C, or in other words for large values of charging current, and are not significant to the final delay value. Equation (14) could be simplified by means of (8), giving:

$$V_{CAPi} = \frac{I_{C0}}{K_N'(V_{DD}-V_T)}(1-mV_C) \qquad (15)$$

where I_{C0} ($=A_I I_{D0}$) is the maximum capacitor charging current.

Figure 5 shows simulated output waveforms for various control voltages (from V_C=0V to V_C=2V with 0.5V step)

for a fall edge of the input pulse. The linear variation of capacitor voltage is in accordance with the assumed constant capacitor charging current, starting from a initial voltage linearly dependent on the control voltage.

Finally, in order to find the delay dependence on physical parameters, we derive the analytical expression for the time needed for the capacitor voltage to reach $V_{DD}/2$ (assuming that the input signal has a fall time much smaller than the delay time and delay measured at $V_{DD}/2$). The time needed for a charging current I_C, given by (12), to produce a capacitor voltage change of ΔV_{CAP} ($=V_{DD}/2-V_{CAPi}$) is:

$$t_{d1} = C\left[\frac{V_{DD}}{2I_{C0}(1-mV_C)} - \frac{1}{K_N'(V_{DD}-V_T)}\right] \qquad (16)$$

which is the equation that models the delay of the current source inverter.

III. Overall Delay

To find the overall delay of the entire non-inverting delay cell, we must add the previously calculated delay (t_{d1}) to the delay of the static inverter (t_{d2}).

The first delay model for the CMOS static inverter which includes the effect of the input waveform was presented by Hedenstierna and Jeppson [8]. They show that for fast input ramps the propagation delay could be written as the sum of an initial delay (proportional to the input rise time) and a final delay (equal to the step delay). Similar results were obtained by Vemuru and Thorbjornsen [9]. The model was generalized by Kayssi *at al.* [10] for exponential input waveforms and Sakurai and Newton [7] introduced the α-power law MOSFET model to calculate the delay for short-channel transistors. Recently, results were extended by Jeppson [6] and Dutta *at al.* [11] to include any value of the rise time of the input ramps.

In this work we use the results of Dutta *at al.* [11] to find the delay of the static inverter over the whole range of input transition-times and fanouts (f_o). The expression that describes the delay is (cf. Eq. 11 in [11]):

$$t_{d2} = \left(-1 + \frac{a}{\tau^b}\right).t_{rin}.D_{slope} \qquad (17)$$

where $\tau=t_{rin}/f_o$ and D_{slope} is the slope of the dc asymptotic approximation of the curves for infinite input rise-times. If D_{slope}, a and b are properly determined, the delay could be accurately found, for a given f_o, if the rise time (t_{rin}) of the input signal were given. Defining t_{rin} as the time to capacitor charge from 0 to V_{DD}, by the current I_C given by (12), we can write:

$$t_{rin} = V_{DD}\frac{C}{A_I I_{DO}(1-mV_C)} \qquad (18)$$

TABLE I
VALUES OF PARAMETERS FOR DELAY CALCULATIONS

Parameter	Value
K_N	5.9
K_N'	17.8
K_P	1
I_{D0}	$260\text{x}10^{-6}$
A_I	3.37
a	$200\text{x}10^{-9}$
b	0.813
D_{slope}	0.055

The overall delay is simply the sum of the individual delays given by (16) and (17).

$$t_d = t_{d1} + t_{d2} \qquad (19)$$

IV. Results

In this section we illustrate the validity of the proposed formulas in the design of non-inverting delay elements for use in voltage controlled delay chains. The results are compared with SPICE simulations using 1.2μm CMOS technology. Some factors must be taken into account before use the derived formulas. Firstly, the capacitor must be large enough relatively to parasitic capacitors in order to minimize the errors due to variations on the latter. The value used in the calculations is 250fF. Secondly, for this technology the square law, long channel transistor model is only approximate, and results do not agree well with simulation (even if non-minimum transistor sizes are used). As a consequence the current gain (A_I) is smaller than the predicted value and the maximum current I_{D0} is not accurate. To overcome this problem we find the approximate transistor dimensions and capacitor value for a given overall delay (t_d) (note that the specifications for t_{d1} can be derived from t_d because t_{d2} can be approximated by results on [11]). Next, a simulation is performed with V_C=0V and the current in M1 and M5 is determined (to give a more accurate value for A_I). We also need to measure the initial capacitor voltage from V_C=0V and V_C=1V (this is a process similar to the method used by Dutta [11] for finding parameters a, b and D_{slope}). With these one-time simulation real parameters can be found for plotting accurate delay characteristics for the initial transistor sizing (see Appendix for derivation of the parameter evaluation). If the overall delay results are not satisfactory simple modifications on transistor dimensions are required. The inspection of the dependence of the final circuit on physical parameters gives a final result in a single iteration. Table I shows the final parameters obtained for a given circuit (note that the K_N's are

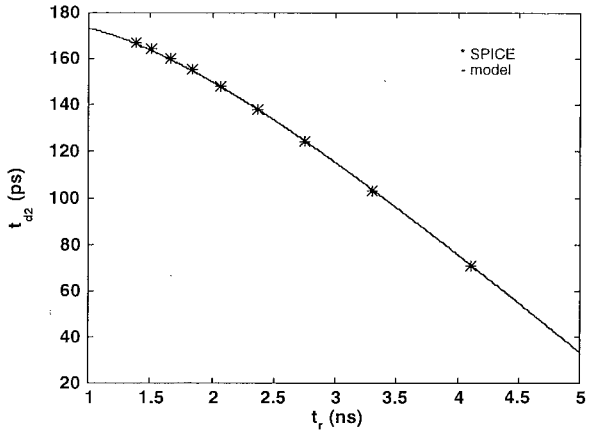

Fig. 6 - t_{d2} plot for f_o=1 (β=W_{M7}/W_{M8}=1).

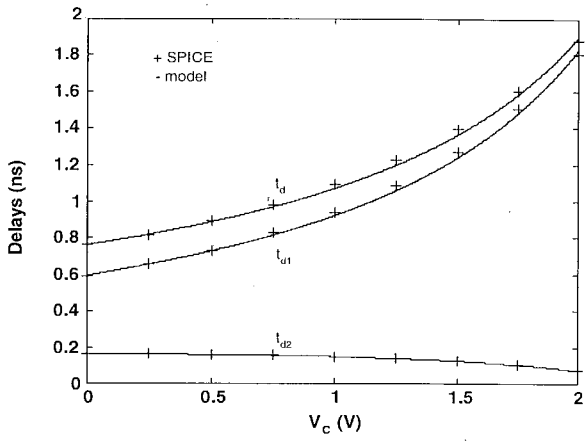

Fig. 7 - Theoretical and simulated delay results.

normalized with respect to K_P), designed for a 1ns delay per cell.

The values of the parameters parameters a, b and D_{slope} for the static inverter are determined by curve-fitting as suggested by Dutta [11] and in Fig. 6 they are shown to be in good agreement with SPICE simulations. The values of t_{rin} used for SPICE simulation are obtained from (18), for V_C's in the range 0-2V.

With the parameters shown in Table I (assuming that V_{TN}=V_{TP}=0.75V), delays t_{d1}, t_{d2} and t_d obtained from (16), (17) and (19) are plotted in Fig. 7. The corresponding results obtained from SPICE are also plotted and show very good agreement with the theoretical formulation.

The differential non-linearity between V_C=0V and V_C=2V is better than:

$$\frac{\left|\left(\frac{dt_d}{dV_C}\right)_{V_C=2V} - \frac{t_{d|2V} - t_{d|0V}}{2}\right|}{\frac{t_{d|2V} - t_{d|0V}}{2}} = 1.7 \qquad (20)$$

This represents a differential non-linearity four times smaller than the obtained with pulse-shrinking buffer for the same variation of delay per cell (cf. [1]).

V. CONCLUSION

Even with the required recalculation of the parameters for more accurate results, the proposed non-inverting delay element shows a quasi-linear voltage controlled delay characteristic which is more suitable for use as interpolating elements in voltage control delay chains as in DLL applications (the gain of DLL is less dependent on point of lock). The analytical expressions are simple and comprehensive and show the dependence of the delay on physical parameters allowing, typically with only one iteration, the calculation of transistor dimensions for a given delay per cell of the delay chain.

APPENDIX

For more accurate results it is convenient to find more accurate values K_N, K_N' and A_I (we assume that K_P=1).

From the equation that describes the charge of a capacitor by a current I_C, we can write for V_C=0V:

$$A_I = \frac{(V_{DD}/2 - V_{CAP0}).C}{t_{d0}.I_{D0}}$$

where V_{CAP0} is the initial capacitor voltage for V_C=0V, t_{d0} is the corresponding simulated delay measured at V_{DD}/2 and I_{D0} is the current through M1 for V_C=0V.

To find K_N, we obtain from (13) (for V_C=0V and V_C=1V):

$$m = 1 - \frac{1-\left(1-\frac{V_{CAP1}}{V_{DD}-V_T}\right)^2}{1-\left(1-\frac{V_{CAP0}}{V_{DD}-V_T}\right)^2}$$

where V_{CAP1} is the initial capacitor voltage for V_C=1V. With the m value we can calculate K_N from (11) assuming that K_P=1:

$$K_N = \left[\frac{m(V_{DD}-V_T)}{2-m(V_{DD}-V_T)}\right]^2$$

Finally, from (13) with V_C=0V, K_N' can be calculated as:

$$K_N' = \frac{A_I K_N}{(1+K_N)\left[1-\left(1-\frac{V_{CAP0}}{V_{DD}-V_T}\right)^2\right]}$$

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