A CMOS SIGNAL TO NOISE MEASUREMENT CIRCUIT FOR INFRARED SECTORED RECEIVERS

Luís Nero Alves, Rui L. Aguiar, Dinis M. Santos

***Resumo* – Este artigo descreve um circuito capaz de medir a Relação Sinal Ruído em sistemas de comunicação por Infravermelhos. A relação Sinal Ruído desempenha um papel fundamental em Receptores Sectorizados por IR, pois é necessária para métodos de selecção ou combinação dos sinais vindos dos diferentes sectores ópticos. O circuito aqui descrito é capaz de estimar a razão entre a potência média do sinal adquirido pelo fotodetector e a potência de ruído presente no mesmo, apresentando uma gama dinâmica de 50dB.**

***Abstract* - This paper describes a circuit able to measure Signal to Noise ratios developed for Infrared applications. The Signal to Noise ratio is of major importance in IR Sectored Receivers because it provides the basis of selection or combining of signals coming from different optical sectors. This circuit estimates the ratio of the average optical signal sensed in the photo-detector and the average noise power present in the same photo-detector, with a 50dB output dynamic range**

I. INTRODUCTION

Due to the emergent wireless LAN technology, and to the promising infrared medium, several efforts have been made in the design of optical receivers [1]. The main aspect of these optical receivers is their "almost" diffuse nature of reception. However, as dominant noise sources are usually fixed (such as illumination lamps, or windows), the optical sensor is preferably composed of several photo-detectors with a small FOV, oriented in different directions. Thus most of the surrounding environment will be covered but some of the principal noise sources will still be avoided. The receiver is then responsible for processing the information from all photo-detectors in order to maximise signal while minimising noise. This is accomplished either as selecting the best optical sector (*Best Sector*); or by combining various optical sectors (*Maximal Ratio*) [2]. This selection/combination is based on the signal to noise ratio (SNR) of each optical sector [3-5]. For a *Best Sector* receiver, the selection is based on the best SNR presented in all the sectors. *Maximal Ratio* receivers produce an output proportional to the weighted sum of the signals of all the sectors, where the weights are the SNRs of each individual sector.

Thus a measure of the optical SNR of each sector is required in both types of sectored receivers. This SNR is proportional to the ratio of the average optical power received to the average noise power present in the photo-detector, $<I_s>/\sigma$. The noise power is $\sigma^2=2qI_{dc}B$, where q is the electron charge, I_{dc} is the DC current component present in the PIN photo-detector due to the various natures of noise interference, and B is the system bandwidth; $<I_s>$ is proportional to the signal power.

II. THE OVERALL CIRCUIT IMPLEMENTATION

The current efforts in the design of IR Sectored Receivers led to the implementation of prototype versions of these systems with discrete hardware. Due to area considerations, any final version should be a low cost, low power ASIC. For cost considerations, this ASIC should be implemented with CMOS technology.

Several implementation strategies were investigated on the design phase of the SNR estimator, which requires a divider. An obvious way to implement analogue division are logarithmic techniques; however, these are not easy to implement in CMOS technologies. Another possibility is the use of translinear circuits [6]. Nevertheless, translinear circuits, although simple and very accurate, do not permit the dynamic ranges pretended and would further exceed the allowable power consumption. (This circuit will be replicated in each sector of the wireless receiver, and thus total power consumption would be much larger than the individual consumption of each SNR estimator.) Some studies were also done around current conveyor concepts and the synthesis of mathematical functions in this domain [7,8]. This approach was abandoned because of the use of MOS transistors in the linear region and of dynamic range limitations.

A more classical approach uses an analogue multiplier and some non-linear feedback concepts; this proved to be suitable for our design [9]. At the heart of this circuit we have three main blocks, two multipliers and one divider. Other circuits presented in Fig.1 are responsible for signal acquisition and conditioning, polarisation and voltage reference. We use differential signal paths in order to increase noise immunity and to increase the common mode rejection ratio. In this way it is possible to (although probably not desirable) to accommodate both analogue and digital processing units in the same chip. Furthermore the front-ends for which this circuit was conceived have differential topologies also.

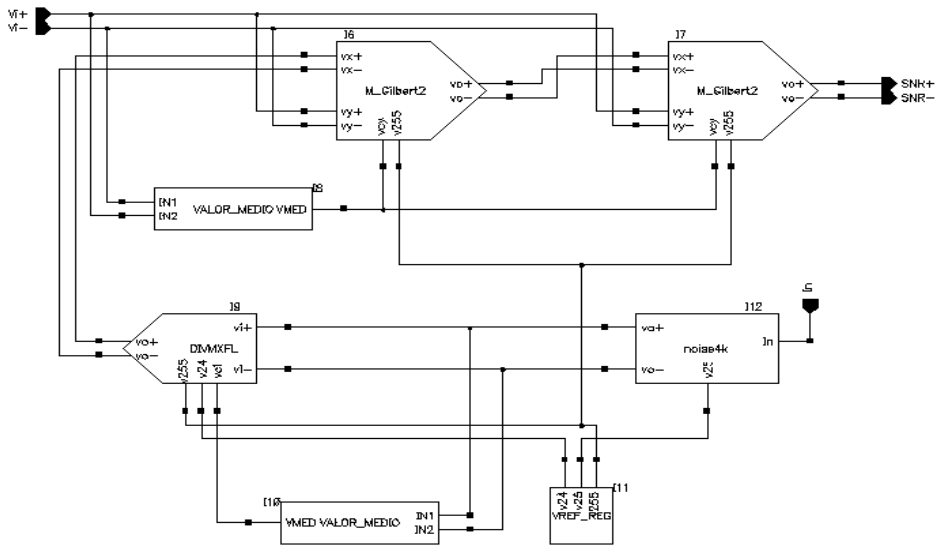

Fig. 1 SNR Measurement Circuit

The first stage, labelled Noise4k in Fig.1 is a simple current to voltage converter, whose principal function is to measure the noise (roughly equal to DC component) in the photo-detector. This circuit has the function of low-pass filtering this noise current also (the cut-off frequency is near 2MHz). The acquired noise signal $\sigma^2=2qI_{dc}B$, is then fed to the divider circuit, in order to perform the $1/\sigma^2$ operation. The next step is the analogue multiplication of this pre-processed noise signal by the output signal of the front-end v_s. We assume to have a linear proportionality between the current signal I_s, at the photo-detector, and the v_s signal (which is reasonable for most front-ends). This multiplication is done twice in order to achieve v_s^2/σ^2, the square of the Signal to Noise Ratio.

There are several reasons to measure the squared SNR and not the SNR itself. First, it is not easy to implement square root extraction circuits for the whole dynamic range we have in infrared applications. Second, if this circuit is to be used in a *Best Sector* receiver, it is desirable to have unipolar quantities to simplify the discrimination step. If the target is a *Maximal Ratio* receiver, this same signal can be applied to a AGC (automatic gain controlled amplifier).

The blocks labelled Valor_Medio are responsible for the polarisation of the multiplier cells. This polarisation scheme is based on actual incoming signals, and makes the circuit more robust and less dependent on signal levels. Finally the block labelled Vref_Reg is responsible for all the necessary voltage references in the circuit. We choose to have these references produced inside the chip so they could be more accurate. The reference circuit is a simple series regulator, capable of a 22% regulation factor.

Not present in Fig.1 is the circuit for low-pass filtering of the final SNR squared result. This filtering is needed to have an average expectation of the optical SNR.

II. THE DIFFERENTIAL MULTIPLIER

The multiplier cell is basically a folded Gilbert multiplier as can be seen on Fig.2. The folded configuration was preferred to the usual form due to its larger dynamic ranges (both at the input and output). The core of the multiplier is composed of transistors NMOS M1 to M4, and PMOS M5 and M6. Transistors NMOS M7 to M10 are used with two purposes: establishing the circuit dynamic polarisation and correcting the quadratic non-linearity exhibited in the fundamental Gilbert cell [10-12]. This way we could achieve a multiplier circuit with high degree of linearity inside the proposed input voltage range (1.5V to 3.5V).

The differential output current is achieved through a cross-connected current mirror. Finally, a resistor and a fixed voltage reference do the current to voltage conversion.

IV. THE DIVIDER CIRCUIT

The divider circuit is a classical example of non-linear feedback theory. Analogue division can be achieved through the use of a multiplier placed in the feedback loop of an operational amplifier, as showed on Fig.3. The design of this circuit was a major problem due to its natural tendency to exhibit oscillations. The compensation was accomplished through the reduction of the bandwidth and gain of the operational amplifier.

V. SIMULATION RESULTS

This circuit was implemented in AMS 0.8μm CMOS double poly, double metal technology, using the Cadence DFII environment and the SpectreS simulator. The following sections show the simulation results achieved.

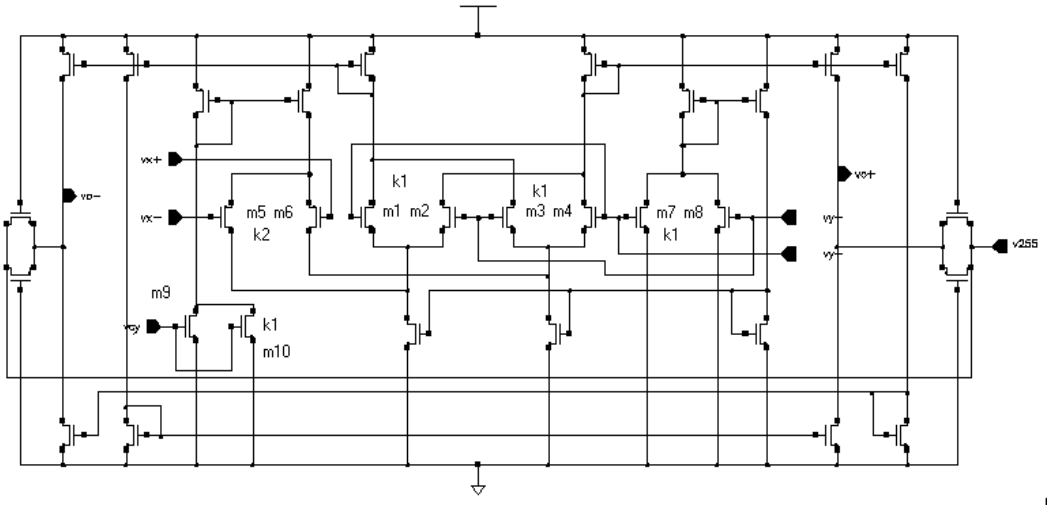

Fig. 2 Differential multiplier based on the Gilbert Multiplier cell

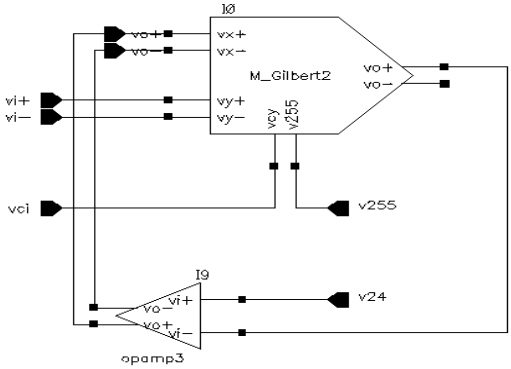

Fig. 3 Divider circuit

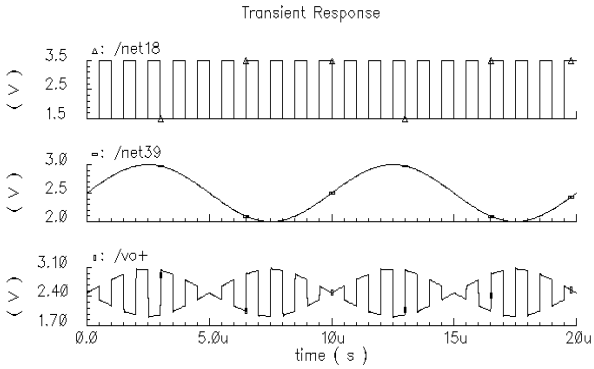

Fig. 4 Multiplier transient response

A. The Multiplier

Figure 4 shows the good linearity of the multiplier transient response. This figure represents the AM product of two waves: a square wave (the carrier) at 1MHz, with amplitude of 1V and offset of 2.5V, and a sine wave (the modulating signal) at 100kHz with amplitude of 500mV and offset of 2.5V. The product of these two waves is an AM signal with almost 1V of amplitude and offset near 2.5V. We should point out that in our target application (keeping this AM analogy) the carrier is the PPM signal at the output of the optical front end, and the modulating signal is the measured average noise present at the systems input.

In Fig. 5 we show both signal excursions, at the input 1.5V to 3.5V and at the output 1.5V to 3.5V. The expected input dynamic range is about 20dB (the output signal from the front end lies in the range of 80mV to 1V with 2.5V of offset). The output dynamic range can span more than 50dB (from ci. 3mV to 1V).

We also measured the rise time exhibited by this multiplier. Both rise and fall times fall in the range of 7ns to 10ns. The circuit bandwidth is always superior to 20MHz, and shows the expected small variations with the input signal amplitude. These values exceed the maximum requirements presented in the wireless LAN applications we targeted.

B. The Divider

The divider DC response is depicted in Fig. 6 where we can see the approximated 1/x function. The input and output excursions are respectively 1μA to 300μA (50dB) and 2.5V to 4V (50dB). The divider's bandwidth is limited to 2MHz. This limit is imposed by two factors: i)it is desirable to have a filtering effect over the measured input noise, and ii) the system may become unstable with larger bandwidths.

C. The SNR Measurement Circuit

Fig.7 shows the overall system performance, when the input signal has constant amplitude, and noise has a triangular periodic pattern. We can see the 1/x function applied to the measured noise (the bell shaped signal), the first product with the input signal and finally the desired squared SNR. The filtering stage necessary to have the average sense of the SNR was not shown because its cut-off frequency depends on the wireless LAN specifications (namely: the type of signal modulation, the type of wireless propagation being used - diffuse or not-, the total

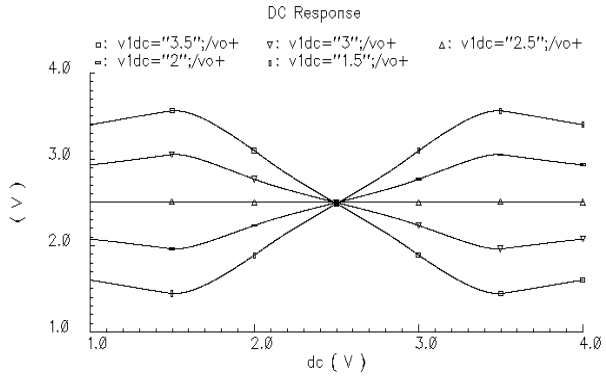

Fig. 5 Multiplier DC response

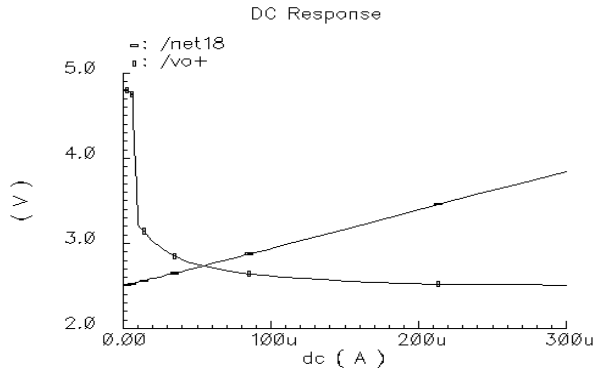

Fig. 6 Divider DC response

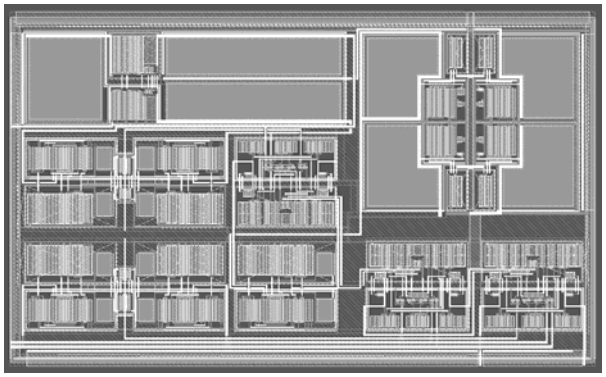

Fig. 8 Circuit Layout (780μm×480μm)

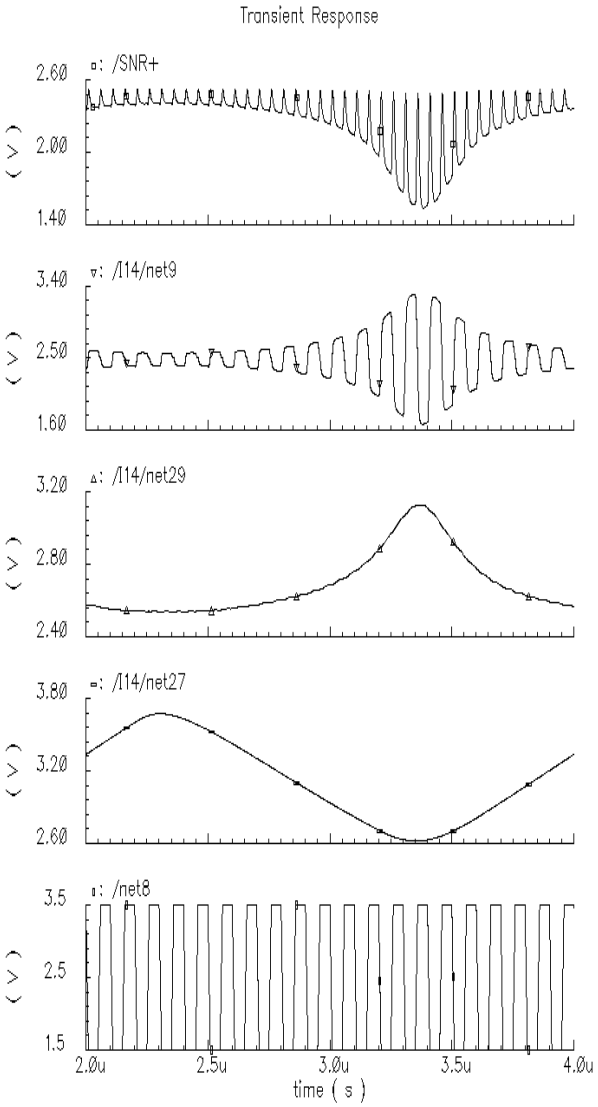

Fig. 7 Overall circuit transient response
(From top to bottom: SNR output signal, first multiplier output, divider output, measured input noise and front end output signal)

network bit-rate and the combining/selection scheme to use).

The circuit was simulated with different models and proved to be robust to process changes. Some simulations were made adding noise to the power lines and with extreme input signals; in these extreme situations the circuit still produced useful outputs.

The power consumption is expected to be in the range of 36mW and the layout area of 780μm×480μm (see Fig. 8). Our target wireless system is being designed with eight sectors, and thus total power dissipation would be in the 250mW range, which is low enough for our purposes.

VI. CONCLUSIONS

This paper describes a SNR measurement system for optical sectored receivers, with a 50dB output dynamic range. This circuit is part of a complex receiver for wireless optical LANs, as described in other papers of this issue. We discussed the basic blocks of the system and several design constraints. The final result is a circuit with a fairly good linear response, implementing the desired function even in extreme cases. The overall power consumption presents reasonably small values for its integration in a multiple-sector receiver.

VII. ACKNOWLEDGEMENTS

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