Electronic Circuits for Wireless Optical LANs - II

Rui L. Aguiar, António Tavares, José Luis Cura, Eduardo de Vasconcelos,
Luis Nero Alves, Rui Valadas, Dinis M. Santos

***Resumo* – Este é o segundo de dois artigos que discutem a implementação de emissores/receptores para redes locais não cabladas utilizando a tecnologia de infravermelhos, de baixo custo. O trabalho aqui apresentado cobre maioritariamente os elementos da camada física.**

As redes locais não cabladas consideradas têm taxas de transmissão entre 4Mbps e 25Mbps, e a capacidade do fotodíodo receptor entre 10pF e 50pF. Os tipos de modulação considerados são tipicamente 4-PPM ou 16-PPM.

Neste artigo são apresentados circuitos relacionados com o problema de receptores sectorizados e com as questões de sincronização e detecção de símbolo. Uma secção final contém alguns dos problemas de evolução destes sistemas de baixo preço.

***Abstract* - This is the second of two papers discussing practical issues and results on the implementation of low-cost transceivers for several wireless optical LANs, covering most physical layer elements.**

Target optical LANs under consideration have bit-rates varying between 4Mbps and 25Mbps, and input photodiode capacitance may vary between 10pF and 50pF. PPM modulation, either in a 4-PPM or 16-PPM format, is typically used in the physical layer.

This paper presents circuits related with sectored receivers, clock recovery and symbol detection. A final section presents some of the problems related with the evolution of these low-cost systems.

I. INTRODUCTION

Wireless optical communication systems have gone through considerable developments in recent years, as optical components have suffered important technologic advances and substantial price decreases. Thus data communications are increasingly using wireless optical systems at higher speeds. These systems are being used as an alternative to cabled media, mainly due to their simpler deployment and reconfiguration.

In wireless optical networks, major hindrance results from the low signal amplitudes that have to be used due to cost, health and power consumption constraints. Furthermore, the non-uniform nature of both the ambient noise and the signal power distribution puts increased demands on the dynamic range of the transceiver circuits. These wireless optical constrains call for new solutions, namely: (i) networks optimized for the usage of low cost optical components, (ii) development of systems with very flexible characteristics of gain and dynamic range, (iii) noise reduction techniques, and (iv) selection of optimal detector structures.

We have been developing wireless optical LAN systems pursuing these objectives. This paper documents some of our efforts in implementing practical low-cost transceivers.

In a first companion paper on the subject we discussed the target WLAN characteristics we used as reference for our work and the system reference block we have followed over the last years. Then we highlighted some issues on emitter design, and an in-depth discussion on the front-ends that we have implemented; both in discrete and integrated format. The overall acronym list is presented in the first paper.

This second paper addresses the sectorization problem in section II. Section III summarises some practical constraints related with the digital recovery of the signal in WLAN transceivers, viz. symbol detection and clock recovery issues. Considerations on overall practical aspects are presented in Section IV, trying to highlight some of problems in designing circuits for WLANs. Our conclusions, mostly as directions for future work, are presented in section V.

Note also that an independent paper on Signal-Noise measurements, also being presented in this issue, is of relevance to this work.

Most of the circuit blocks reported here have already been tested in various generations of working prototypes (with varying specifications). More recent work is currently under field test to assess its performance. Nevertheless, our current activity is focused on cooperative usage of these different circuit blocks, in order to provide efficient WLAN communications.

II. DIVERSITY RECEIVER

Receivers for IR communication systems are usually based on a single optical detector. This is a good configuration in environments where both signal and noise are isotropic. However, in most environments the transmitted signal illuminates the receiver from privileged directions. Also, the ambient light noise emanates from particular directions coinciding with the position of lamps or windows. Moreover, these light sources are frequently in the receiver field-of-view (FOV). These characteristics cause large variations on the SNR, depending on the position, orientation and radiation pattern of both signal and noise sources and on the position, orientation and FOV of the receiver.

To minimise the effects of SNR fluctuations, several receiver techniques were proposed [e.g. 10,31,27]. [10] suggested an adaptive data rate receiver, where the data rate is continuously adjusted with the purpose of maintaining full network connectivity, trading-off speed

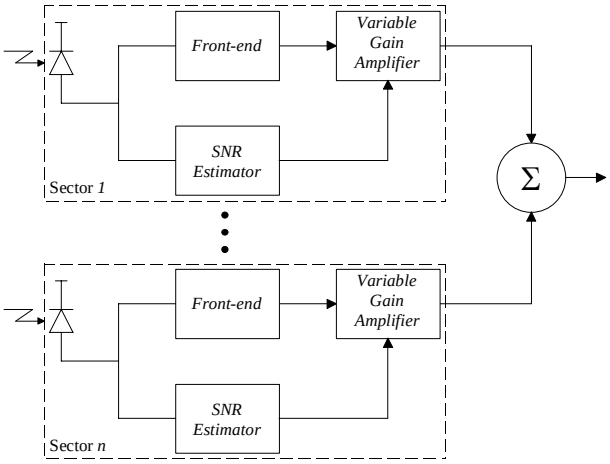

Fig. 1 - Structure of a maximal-ratio diversity receiver.

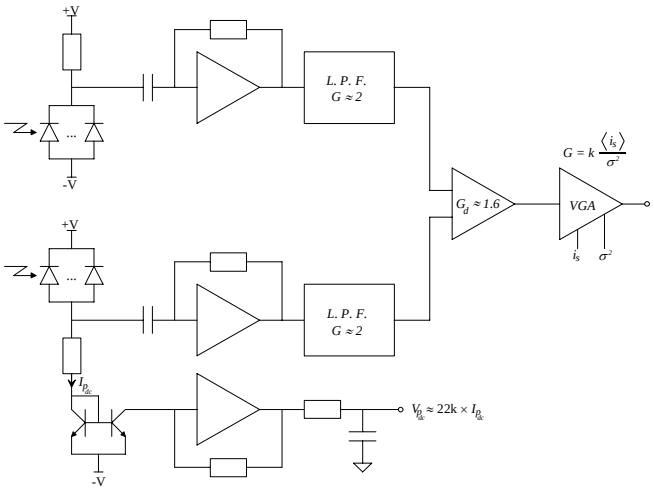

Fig. 2 - Block diagram of one sector.

and range. [31] proposed the use of an angle-diversity receiver who was shown to reduce significantly the optical penalty induced by ambient noise [29]. More recently, [27] studied the combined use of multi-beam transmitters and angle-diversity receivers, based on a single imaging concentrator coupled with a segmented photodetector, showing also significant optical gains. Angle diversity showed, also, to be very effective in combating multipath dispersion [18].

An angle-diversity receiver is composed by multiple sectors (optical receivers) with a relatively small FOV. Each sector estimates the SNR of the collected signal. With *Best Sector* receivers only the sector with the best SNR is selected. This contrasts with the case of a *Maximal-Ratio* receiver, where the output signals of all sectors are combined through an adder circuit, and each output signal is proportional to its respective SNR.

A way of implementing maximal-ratio system is to put the gain of a sector proportional to i/σ^2, where i and σ represent the average signal and noise root mean square (*rms*) values, respectively. This structure of a maximal-ratio angle-diversity receiver is illustrated in Fig. 1. The receiver comprises one front-end, one circuit to estimate the SNR and a variable gain amplifier (VGA) per sector. The output signals of all sectors are combined through an adder circuit.

For a best sector receiver, a simpler signal selector would be used, without the need for the VGA (see Fig. 4). The data signal would be selected in function of the best SNR.

A. Discrete Implementation (Maximal-Ratio)

The goal of the implemented maximal-ratio angle-diversity receiver is to reduce the penalty induced by stationary photocurrent arising from ambient light sources. Our implementation ignores the optical interference produced by artificial light. The assumption of a stationary quantum noise is the major limitation of this implementation. Although during the bit slot time the quantum noise could be considered stationary, it could vary significantly during the interference period. During the design of the optical sector, it was assumed that the penalty associated with the optical interference could be reduced through the utilisation of an appropriate encoding method, along with adequate electrical and optical filtering [19,21].

In addition to thermal noise, shot noise and optical interference, there is another signal degrading factor as discussed in the companion paper: EMI. To reduce EMI effects, each sector of the infrared receiver was separated in two complementary low noise transimpedance amplifiers, as discussed before. The design of the optical front-end followed the one presented by [28], and was designed to operate at 1Mbps using Manchester line coding. A block diagram of the IR receiver is shown in Fig. 2. Each sector includes two arrays of PIN photodiodes (in this case we have used configuration A (Fig. 2 in the companion first paper), for simpler front-end design), two differential low-noise transimpedance amplifiers and a differential amplifier (as discussed in the first part), but now this is followed by a VGA. The purpose of this VGA is to exhibit an output signal proportional to SNR^2.

The gain of each sector in this maximal-ratio receiver must be proportional to the relation i/σ^2, and can be described by

$$G = k\frac{\langle i_S \rangle}{\sigma^2} \qquad (1)$$

where $\langle i_s \rangle$ and σ^2 are the average desired signal and the shot noise mean square values referred to the input of the front-end, respectively; k is a scale factor characteristic of the receiver. Thus, the signal amplitude obtained at the output of each sector is proportional to the square of the SNR and can be given by

$$V_{S_o} = k\left(\frac{\langle i_S \rangle}{\sigma}\right)^2 = k \times (\mathrm{SNR})^2 \qquad (2)$$

The variance of the input-referred noise (shot noise), accounting the pulse shaping after the preamplifier, is

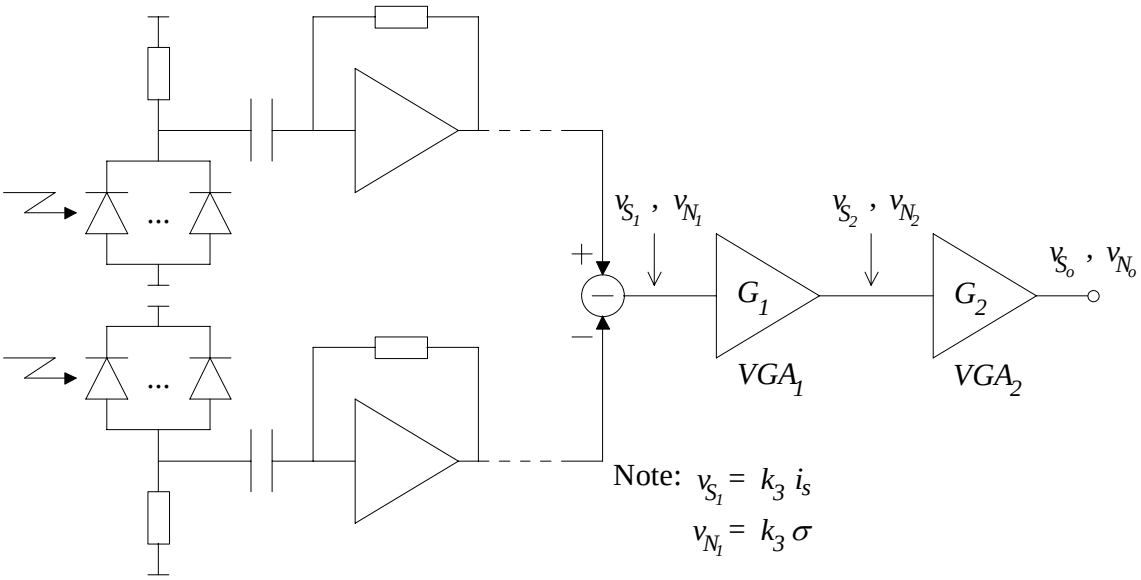

Fig. 3 - Block diagram of one sector with two VGA's.

proportional to the average value of the DC photocurrent $I_{p_{DC}}$ and is given by

$$\sigma^2 = 2qI_2 I_{p_{dc}} B \tag{3}$$

where q is the electronic charge of an electron, B is the bit-rate and I_2 is a noise bandwidth factor depending of the transmitter pulse shape and equalised pulse shape only. For our receiver implementation $I_2 \approx 0.56$. As the shot noise mean square value is proportional to the DC photocurrent, the gain of the VGA, represented by equation 1, can be given by

$$G = k\frac{\langle i_s \rangle}{I_{p_{dc}}} \tag{4}$$

To implement the desired gain it is necessary to evaluate $I_{p_{DC}}$. Since the complementary photodiode arrays are placed near enough, the DC photocurrent induced on both photodiode arrays is almost identical. So, $I_{p_{DC}}$ measurement can be done on one branch of the differential front-end only. Fig. 2 illustrates the evaluation of $I_{p_{DC}}$, which was performed through the inclusion of a current mirror into the photodiode bias circuit.

When designing the VGA it must be taken into account that the optical transmission channel has a large optical range both in terms of signal and noise. These characteristics demand a large dynamic range for the VGA (its gain may need to vary in a large range). Indeed, a series of measurements of PD density presented in [28] showed that, in typical well-illuminated environments, the DC photocurrent induced in a PIN photodiode could vary between 12μA/cm^2 and 1.2mA/cm^2. Assuming signal irradiances with an electrical dynamic range of about 40dB, the required dynamic range of the VGA equals 60dB, which is difficult to implement. This problem can be relaxed through the utilisation of a cascade of two VGAs. Fig. 3 illustrates this option and identifies some signals used during the design of the VGAs.

Now we have to decide on which gain should be assigned to each VGA. As the VGA is controlled by two distinct signals, $\langle i_s \rangle$ and $I_{p_{dc}}$, the easiest option would be to have $G_1 = k\langle i_s \rangle$ and $G_2 = k/\sigma^2$, where G_1 and G_2 are the gains of the first and of the second VGA, respectively. However, this option still requires a large VGA dynamic range. In fact, the required VGA dynamic range would be of 30dB in each VGA. An alternative is to define

$$G_1 = \frac{k_1}{\sigma} \tag{5}$$

and

$$G_2 = k_2 \times V_{S_2} \tag{6}$$

where V_{s_2} is the amplitude of the signal at the input of the second VGA. This option is more complex because it requires a square root circuit for $I_{p_{DC}}$ but, as we demonstrate, the obtained profits compensate the complexity. With this implementation, the dynamic range of the first VGA (VGA_1) will be below 6dB, which can be easily implemented. Then, the average output signal of VGA_1, $\langle V_{s1} \rangle$, will be proportional to the SNR

$$\left\langle v_{S_2} \right\rangle = \langle i_S \rangle A_{FE} G_1 = k \cdot SNR \tag{7}$$

where A_{FE} is the front-end gain. Obviously, the shot noise *rms* value at the output of VGA_1, $\langle V_{N1} \rangle$, will be the same for all sectors

$$\left\langle v_{N_2} \right\rangle = \sigma A_{FE} G_1 = k \tag{8}$$

In the particular situation where all the branches of a maximal-ratio sectored receiver have the same input noise the ideal gain in each sector must be $G = k\langle i_s \rangle$. Since these conditions happen at the input of the second VGA (VGA_2) it is obvious that the gain of VGA_2 must be proportional to the amplitude of its input signal, as given in eq. 7. In other words, the gain of VGA_2 is proportional to the SNR. So, the required dynamic range of VGA_2 is only limited by the maximum and minimum SNR that will be reasonable to consider. In optical transmission systems it is usual to define the receiver sensitivity, as the minimum irradiance required to achieve a BER of 10^{-9}. In our receiver this BER corresponds to SNR=6/√2 (referred to one input of the differential front-end). We will use this value as a reference value during the design of the second VGA. For a SNR double and half of the reference value, the corresponding bit-error rate is about 1.8×10^{-33} and 1.3×10^{-3}, respectively. These values can be considered large and small enough to define the maximum and minimum SNR where the gain of VGA_2 must increase linearly with the SNR. Thus, the gain of VGA_2 must increase linearly from SNR=3/√2 until, at least, a SNR of about 12/√2 resulting in a dynamic range of about 12dB $\left(20\cdot\log\left({SNR_{MAX}}/{SNR_{MIN}}\right)\right)$ for the second VGA.

Finally, through the utilization of the cascade of the two VGAs, the global gain is described by:

$$G = \frac{V_{S_O}}{\langle i_S \rangle} = \frac{G_2 V_{S_2}}{\langle i_S \rangle} = \frac{k_2\left(G_1 V_{S_1}\right)^2}{\langle i_S \rangle} = \frac{k_2\left(\frac{k_1}{\sigma} k_3 \langle i_S \rangle\right)^2}{\langle i_S \rangle} = k\frac{\langle i_S \rangle}{\sigma^2} \quad (9)$$

as required and described in eq. 1. In eq. 9, V_{S1} is the amplitude of the v_{S_1} signal.

B. Integrated System: Best Sector

The approaches leading to the implementation of the diversity receiver were quite different in the integrated and the discrete version.

The key differences were related to power consumption in the context of switched-gain front-ends. The complex structure used for the discrete version would use too much power, when integrated with a switched-gain front-end. (The structure described before will have to be replicated per sector).

Thus we implemented an integrated Best-Sector receiver,

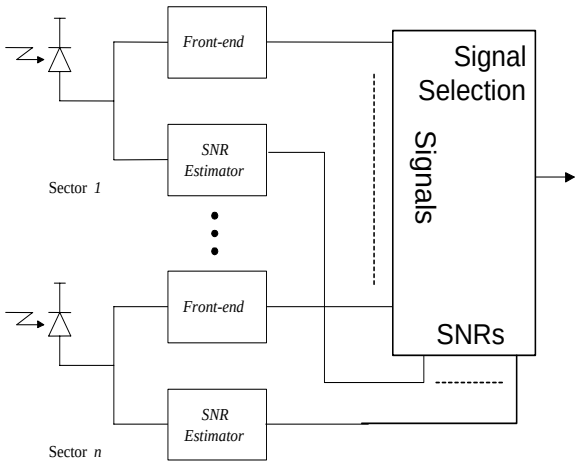

Fig. 4 - Best sector receiver.

as presented in Fig. 4. Although the signal selection unit can require some careful design in the case of switched gain front-ends, the real issue is the estimation of the SNR. Note that in the previous case, no real SNR was estimated directly, but the VGAs had gains such that the final output signal was proportional to the sector SNR.

In this receiver, a variation of the folded cascoded FE was implemented. Furthermore, we implemented a "true"-SNR estimator through analogue processing. The most complex issue in this implementation is the analogue division required. Several techniques can be used for this task [4], and are summarized in Table 1.

Fig. 5 represents the schematic of the circuit implemented (discussed in detail in [4], in this same issue), after several trade-offs have been analyzed.

At the heart of this circuit we have three main blocks, two multipliers and one divider. All the periphery circuits presented in Fig. 5 are responsible for signal acquisition and conditioning, biasing and voltage reference. Differential signal paths are used in order to increase noise immunity and also to allow for better rejection of the common-mode components of the signal. In this way it is possible (although probably not desirable) to accommodate both analogue and digital processing units in the same chip. Furthermore, the front-ends for which this circuit was conceived also have differential topologies.

Table 1 - Analogue division techniques

	Pros	**Cons**
Logarithm conversion	Easy to implement the division	Complex implementation in CMOS of log functions
Translinear circuits	Simple and accurate	Large power consumption, low dynamic range
Current conveyor techniques	Current domain, low noise	Low dynamic range, low design precision
Analogue multiplier and non-linear feedback	Reasonable power, repetitive design	More prone to instability

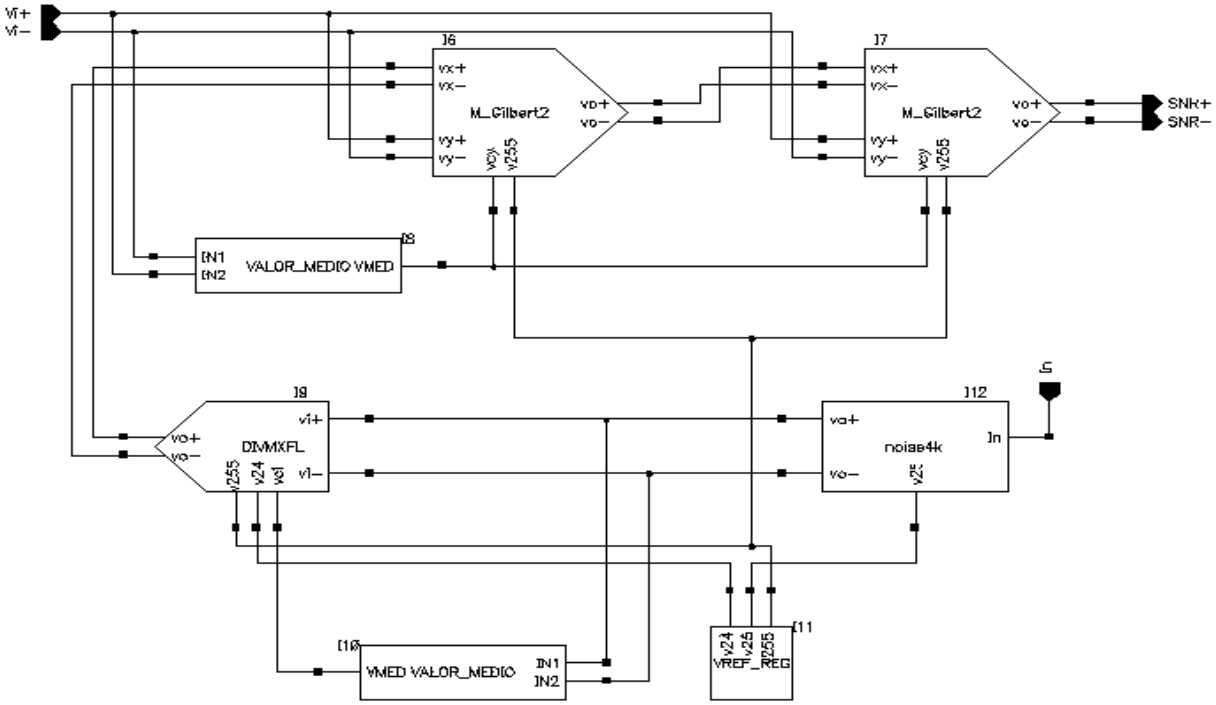

Fig. 5 - SNR Measurement Circuit

Not shown in the figure is the circuit for low-pass filtering the squared SNR result. This filtering step is necessary to provide an average expectation of the optical SNR (its conception is constrained to the type of selection/combining required, the type of signals to handle (PPM, NRZ…), and the type of front-end to be used (fixed gain or switched gain). Note that if non-switched gain front-ends are used, this approach can also be used for a maximal-ratio receiver. The introduction of gain changes in the front-end brings an extra layer of complexity to the system, and thus we decided for the implementation of a simpler best-sector receiver.

Our implementation of the divider circuit follows non-linear feedback theory. The circuit was designed in a 0.8µm CMOS technology, and has been submitted for fabrication [4].

III. DIGITAL SIGNAL RECOVERY

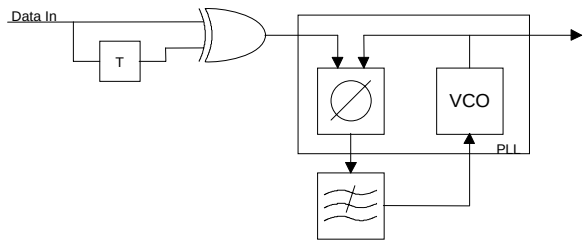

Fig. 6 - Block diagram of the discrete clock extractor.

A. Clock Recovery

We have developed several sub-systems for clock recovery. The most used approach in discrete implementations is a PLL with a very narrow bandwidth. Figure 6 shows a simplified block diagram of the implemented PLL. This approach has been used with Manchester and PPM codes. Naturally PPM clock recovery is more complex than Manchester, but nevertheless this is feasible for the less than 10Mbps networks we have developed.

A clock recovery system was designed to extract an 8MHz clock from a 4-PPM encoded data operating at 4Mbps. This PLL took about 2.5µs (20 slots) to lock the recovered clock with the emitter source. The measured jitter was about 20%(of the clock period) when the data signal was directly applied to the clock extractor.

For an integrated system, we have opted by a PLL with a Hogge phase detector. The clock recovery system we are currently using is represented in Fig. 7. The Hogge phase detector is a digital system, avoiding the extra complexity of analogue non-linearity processing in the PLL (see also section III.B). This phase detector already provides retimed data information, which may be used for word boundary detection and proper MAP detector control.

This clock is divided (in the case of PPM modulation) in order to create the bit and word clocks. These clocks are synchronized in function of the preamble, and of the start of packet detection. Note that other synchronization approaches (such as [15]) are not practicable, as they require a certain number of words to be received before

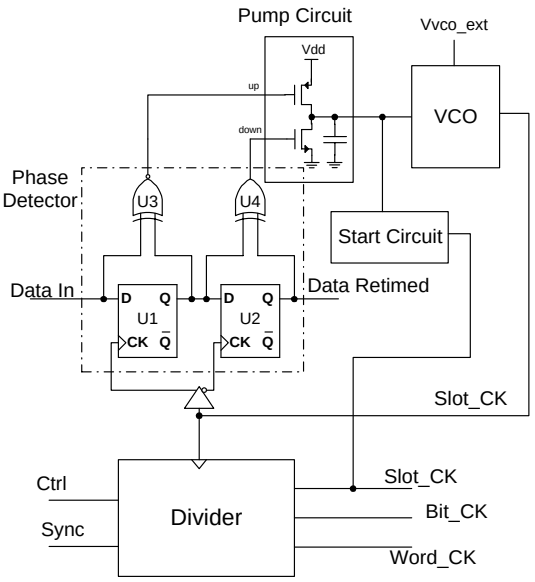

Fig. 7 - PLL with Hogge phase detector.

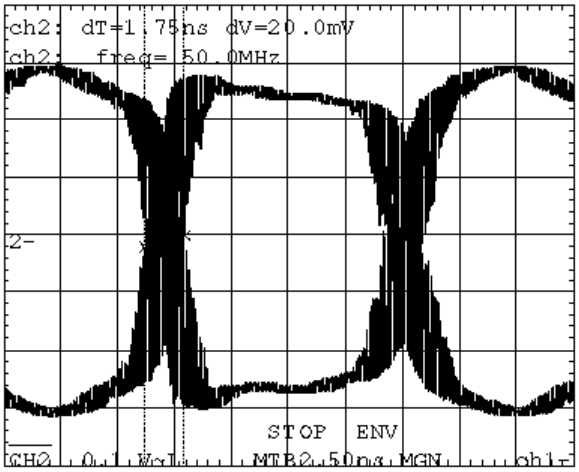

Fig. 8 - Recovered clock after font-end amplification of a 16-PPM signal.

providing a reliable synchronization signal: this is impracticable in a packet-based network.

Key design aspects in clock recovery for wireless optical systems, especially with PPM modulation, are the narrow lock range and fast acquisition times required. The clock recovery system implemented uses as VCO a rail-to-rail inverter-based ring oscillator. The lock range has been carefully trimmed in order for the system to be able to support parameter variations, and still keep a narrow lock range. This is achieved through separate controls in the ring oscillators' starved inverters. Furthermore, some external control is possible, further decreasing lock time, as some of the starved inverters have an external control point. Nevertheless, a simple start-up circuit has been included for faster lock time, even when no outside control is performed.

We have tested this clock recovery system with several bit-rates, ranging from 6 MHz to 60 MHz, integrated in a receiver. Its performance is clearly adequate inside this range, with peak-to-peak jitter below 20% with random 16-PPM signals. Fig. 16 presents such an example of the recovered clock at 50 MHz, when used in a receiver with an integrated front-end, with 30KΩ gain [5]. When data signals were directly applied to this clock recovery unit, jitter decreased to values below 15%.

B. Symbol Detection

Symbol detection is usually as complex as the complexity of the line code being used. In this section we will focus on PPM detection, as the per-election code for WLANs.

Three main types of symbol detection can be generally used: threshold detection, adaptive threshold detection and maximum-a-posteriori (MAP) detection. Threshold detection is simple to implement, but usually does not provide detection quality for realistic environments. Thus only two types of PPM detection are ordinarily considered in theoretical analysis: adaptive threshold (AT) and MAP — sometimes referred to as maximum likelihood, as PPM word statistics are usually assumed equiprobable. The optimum detection method for PPM, even in the presence of noise (and interference) is a MAP approach [21,23]. For instance, typical gains of MAP over AT techniques are better than 1.5dB in WLANs without noise; when ambient noise and interference is considered, this gain increases [21]. This is directly converted into increased WLAN coverage.

Regardless of these considerations, traditional PPM detection is performed by threshold comparison. Simpler approaches use direct threshold detection, while more elaborate ones resort to previous filtering of the signal. Independently of these details, global performance always depends strongly on the way the comparison level is set. Typical approaches for level adjustment range from a manual external adjust (worst performance), going through fixed level comparison [8] and adaptive threshold [22]. Improvements in the performance of threshold level systems are normally possible with the introduction of a good quality AGC amplifier before detection. But even with adaptive threshold and AGC circuits, real systems are not able to reach the theoretical limits for AT performance.

Better performances are generally possible with MAP detection. In PPM systems, a MAP detector decides on the symbol received by making a correspondence to the time slot where more energy has been measured. In order to do this, the detector integrates the signal over each slot, and after sampling all the slots in the symbol, decides that the transmitted symbol is the one that corresponds to the time slot with the largest energy value.

The classic approach to this algorithm would lead to the implementation of an analogue peak detector with multiple inputs, one for each slot. Thus, for a M -PPM code, a typical system would require M (integrating) sample-and-hold (S/H) circuits, and $M(M-1)/2$ two-input comparators; their outputs would be connected to a M-output digital encoder. MAP detection is not usually found

in real systems due to the large number of components and the complexity of this approach.

A completely different approach for PPM detection, used in DSP based systems, resorts to A/D conversion of the received signal. Each slot is digitally converted as received (by an ADC) and digitally stored in a register; at the end of the PPM symbol, these digital samples are processed in order to determine the received symbol. With a proper ADC, with varying conversion levels, this approach may provide interesting practical results, especially if oversampling and posterior digital processing is done. Major drawbacks are the trade-offs in the A/D converter itself (power consumption vs. silicon size vs. speed) and the digital filtering circuitry required after the conversion. These effectively limit this approach to low bit-rates.

We have developed an alternate analogue-digital architecture that implements a very simple MAP detector [1], theoretically providing the same performance as the ideal MAP implementation with much less silicon area and complexity. The MAP detector is schematically represented in Fig. 9 (in the figure, only the lines in bold convey analogue signals). This architecture simply requires a comparator, two S/H circuits, and some digital logic (a register and some control gates) to implement a MAP approach, and thus to achieve the best possible performance. An efficient implementation of this architecture requires the development of an integrated circuit, due to the extremely low signal levels possible in optical systems. Otherwise electromagnetic interference and noise will impair the efficient operation of the circuit.

This detector architecture improves on the classic approach by using a differential strategy, a sample is immediately compared with the "largest value found in a slot"; a digital register always keeps track of the slot number this value was detected on. At the end of the symbol, this register holds the decoded PPM word, that is then stored in a latch. At the same time a reset is made to the S/H circuits, restarting the process. The complexity of the classic approach is thus offset by the processing speed of the digital logic and by a more complex mixed analogue-digital design methodology.

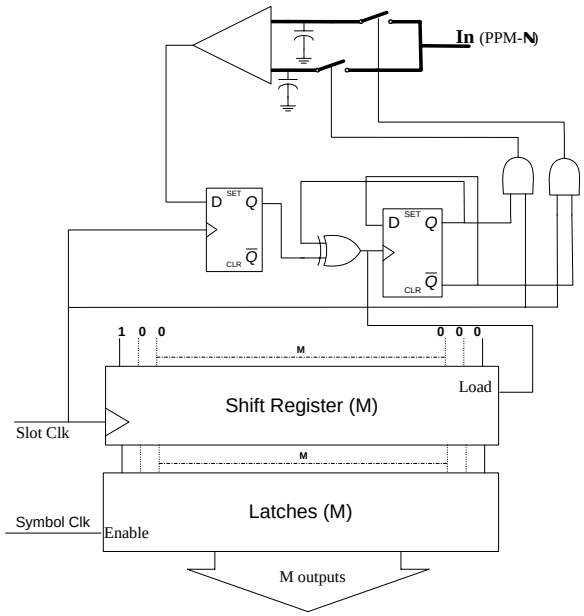

Fig. 9 - Block diagram of analogue/digital MAP detector.

This architecture can be used with any PPM variant that fulfils two conditions: only one pulse is transmitted for each encoded symbol; and all symbols have a fixed length. The behavior of the architecture is indifferent to the PPM order being used, as long as the synchronization clocks are coherent with the modulation order.

We have used this detector in an already mentioned integrated receiver [5]. Circuit problems were detected due to the mixing of digital and analogue signals, and to the fact that there are unavoidable connection lines crossing the blocks (due to the architecture itself). Fig. 10 shows (top to bottom) the analogue signal at the detector input, the recovered clock signal and the word clock signal. Noise levels in excess of 100mV were present even in the power supply lines. This noise is introduced by the clock recovery circuit in the analogue signal and compromises the resolution of the circuit. For instance, the clock recovery circuit only works properly for input currents such that front-end output is better than 120mV. The situation is slightly worse with the PPM decoder, which requires about 140mV at the output of the front-end to decode the input signal with negligible errors. This is due to the fact that this clock-induced noise is greater when all circuit clocks switch, *i.e.* when the word, bit and slot clock are switching simultaneously. In 16-PPM this happens once each 16-slot period. This larger noise affects the analogue signal, and introduces occasional errors in the decoder for values below the mentioned 140mV.

These problems can be minimized by two sets of measures: i) better power supply noise filtering, and ii) usage of differential circuits in the clock recovery unit.

Table 2 summarizes the comparative advantages of the several PPM detection methods discussed.

A further problem related with the usage of MAP detectors is the need for a separate detector for clock

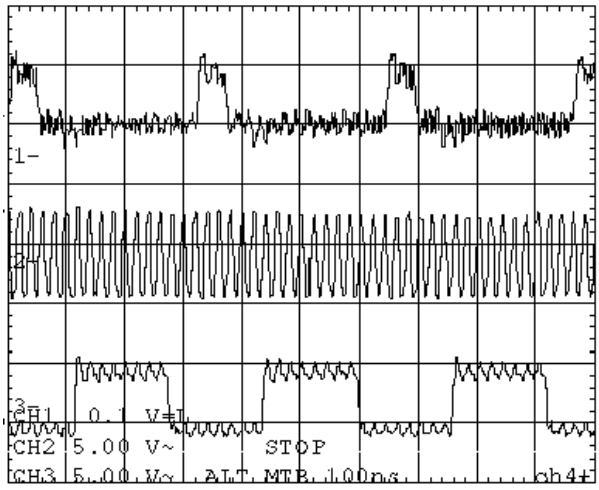

Fig. 10 - Noise in a prototype monolithic receiver (data signal width increased for visibility).

Table 2 - Detector strategies

	Fixed threshold	**Adaptive Threshold**	**DSP**	**MAP (classic)**	**MAP (A/D)**	**MAP (A/D differential)**
A/D	Analogue	Analogue	Digital	Analogue	A/D	A/D
Complexity	Basic	Basic+	High	Medium	Medium	High
Requires integration	No	No	Yes	No	Yes	Yes
Area size	Small	Medium	Large	Large	Medium	Medium+
Power Consumption	Very Low	Low	Large	Large	Low	Medium
Max Bit-Rate	Very High	Very High	Small	Very High	Very High	Very High
Quality	Low	Medium+	High	High	Medium+	High

recovery. If digital phase detectors are used (as discussed in III.A), and then a digital signal has to be delivered to the input of this phase detector. As MAP detection requires the previous synchronization of the several PPM clocks (otherwise the required digital processing is overly excessive), a different detector is required in the input of such a clock recovery system. In practice this implies that the designer has to implement an adaptive threshold detector as input to the clock recovery system. It is then questionable whether the usage of a MAP detector compensates the extra development effort required for a high-quality system.

C. Digital Processing

The implementation of the digital processing at the receiver can also be divided in three aspects:

i) Line decoding (which is trivial),

ii) Un-framing of the information (which we have implemented in an ASIC [2], although current CPLD technology suffices for our target bit-rates in a low-cost implementation) and

iii) FEC decoding.

The un-packetization has a single subtlety, namely the packet fields may carry control information, requiring changes in the receiver behavior (e.g. the data rate field in the 802.12 networks will change the behavior of the receiver to handle 1Mbps or 2Mbps data streams). This brings current real-time control techniques into the design of the whole transceiver. This is especially relevant, as power consumption considerations require these blocks to be usually in a sleep mode, starting immediately upon the reception of a packet.

The issue of FEC decoding is still a pending issue in the development of our networks. We are currently targeting to implement a fully programmable Viterbi decoder.

Our current expectations show that this unit will be by far the largest block to be implemented in the whole receiver, and thus a careful assessment of its real performance benefits and the flexibility degree of such a device have to be concluded prior to its implementation. Nevertheless, this block is still implementable in a CPLD, although it will require a large device.

Experimental results of the BER improvements achievable by the usage of different FEC methods are still pending.

IV. PRACTICAL ASPECTS

Cost issues are a key constraint for WLAN wide-deployment. Transceiver cost is a major part on this problem. While some approaches for transceiver designs require the implementation of complex lenses (eg. [16]), our efforts were centered on electric-related issues. Naturally, better optical approaches should improve on the performance of our networks.

LED prices are already quite low, so the key cost issue is related with the PIN photodiode. Low-cost PDs have small active areas (and thus for large sensitivity systems, several PDs will have to be used) but present reasonably large junction capacitance. This factor places the dominant cost issue on the infrared transducer and on the transceiver circuitry. As mentioned in the companion first paper, these characteristics of the transducer will limit the relationship between network bandwidth, emitted power and cell size.

All electronic processing has been developed with CMOS technology, both for the analogue and the digital sub-circuits — precisely due to the low cost of this technology. As we have shown, the electronic sub-blocks can implement (given some constraints) baud-rates until 50Mbaud, which makes feasible low-power, low-cost 25Mbps networks with 4-PPM coding.

On the electronic processing discussed, the key constraint was related with the FE characteristics. Its design is inherently complicated by the unwanted characteristics of the input PD junction capacitance. Low noise amplification, with high bandwidth and high gain, would be a hard design problem, even without the PD problems. Additionally the large dynamic range required, due to the possible power variations inside the rooms, places another design problem to FE design.

Another critical issue in real systems is the impact of EMI in these very high sensitivity front-ends. EMI is pervasive across the whole circuit, from the power supply contacts to the input circuit pins. High common mode rejection ratio circuits are required, placing another extra burden to FE design. Furthermore, extreme care in the differential signal propagation is required. (Ideally, the PIN photodiodes should be placed in the same substrate than the LNA. A plastic lens (perhaps metal coated) would be applied above this substrate. This would reduce EMI, but its effects on circuit noise are unknown at this moment).

Table 3 - Power budget

		Idle	Peak power
Front-end	full-custom	30 mW	30 mW
SNR estimation	full-custom	30 mW	30 mW
Diversity combination	full-custom	<5 mW	<5 mW
Total for N=8 sectors:	full-custom	~480 mW	~480 mW
Clock recovery circuit	full-custom	30-50 mW	30-50 mW
Word Detection	full-custom	~0 mW	< 10 mW
Word Decoding	full-custom	0 mW	5-40 mW
Analogue/digital ASIC	full-custom	~ 500mW	~ 550mW
LEDs (400mW optical)	16 LEDs	~ 0 mW (off)	~ 3 W (sending)
PINs		< 5 mW	< 5 mW
Digital Packet Processing	CPLD	0 mW	~0.3 W
FEC coding/decoding	CPLD	0 mW	~3 W (receiving)
System interface	CPLD	~10 mW	~0.3 W
Grand Total		~500 mW	~4.5 W

Nevertheless current low-cost technology seems to be able to achieve noise values in the ~10pA/√Hz range, with transimpedance gain* bandwidth products higher than 20THzΩ. This — together with the above-mentioned PD characteristics — imposes a trade-off rule on the network characteristics, in terms of bandwidth and sensitivity. Generically, it seems that this approach may be usable above 100Mbps range (although probably not with simple diffuse networks, but with more complex approaches, such as multi-spot diffusion), a value usually presented in current simulations as one of the limits for wireless networks.

These bit-rates seem to be achievable only through the resort to diversity receivers. But the sheer size of a sectored receiver precludes its practical implementation in discrete form. Integration is a major consideration for the practical development of WLANs. Thus all the electronics will have to be integrated, eventually in a multi-chip ASIC: monolithic circuits are required. This brings an increased layer of complexity to WLAN design and prototyping, leading to more complex systems, with higher power consumption.

Our initial approach to WLAN development was oriented towards a single chip receiver. Some of our results [5] indicate that this approach, if not unfeasible, involves very complex design issues in terms of the electronics, as we have discussed. We currently are targeting a multi-chip ASIC, with an analogue chip (probably associated with a clock recovery system), and a full digital circuit, covering the whole digital processing required for the network. Note that the usage of a MAP decoder can be questionable, as we have discussed in section III.B.

From the considerations presented in previous sections, and from our experimental data, a complete diversity receiver would have a power budget with high peaks on the order of 4.5W distributed as shown in Table 3. Note that this value is very dependent on three aspects: i) the network bit-rate, which will require increasingly larger clock frequencies as bit-rates increase; ii) the usage of CPLD devices; iii) the power efficiency of the LEDs. Furthermore, notice that this is peak operating power: careful power management would place most of the system in a dormant stage most of the time.

The latter issue of CPLD devices is the largest electrical power limitation in the system. It is possible to implement the digital processing in an ASIC [2], which will have a much smaller consumption (rough estimates lead to values between 400mW and 800mW). However, the development facilities provided by CPLD technology makes it a technology of choice for prototype implementation. In a final version, a new ASIC could be implemented, incorporating these facilities. In such a system, power consumption while receiving could be easily reduced to around 1W (and around 3.5W while sending). Furthermore, idle state dissipation would be in the 0.5W range, as table values seem to indicate. Note that these values are achieved without special low-power design methodologies. Commercial systems could present values below these.

V. CONCLUSIONS: OUR QUESTS FOR THE FUTURE

In this paper we discussed some issues related with sectored receivers and the digital symbol recovery in WLANs.

During the two-papers on this issue we showed that key blocks for the implementation of wireless IR transceivers can be done with low-cost electronics, and still achieve high-performance results. The convenient choice of network options (such as emitter radiation pattern, FEC and angle diversity), coupled with specially designed hardware, will allow the implementation of simple, low-cost and high performance physical layer for IR networks. Current technology seems to support foreseeable developments in WLANs.

Thus our conclusions are centered in the network we are seeking to implement in the near future.

The network we envisioned is a packet-base, diffuse network, with FEC. Packet structure will have to be

carefully considered in order for a low frame error rate to be achieved, and is part of our current work.

The network transceiver will closely follow the diagram of Fig. 2 of the companion paper, using sectored receivers. For the same generic transceiver, the relationships between the cell size, transmitted power and bit-rate will be chosen according to the specific application in mind, and few modifications should be required in the basic electronic circuit structures. Our current target is the implementation and trial of a 4Mbps network, over a 5m radius, with 400mW emitter optical power. FE input signals would be in the 100nA-100μA range. However, we expect all the electronics to be immediately adapted to larger bit-rates (10Mbps and 25Mbps) with small increases in transmitter power and/or decreases in cell radius. This would create an environment where the different trade-offs in network design (frame format, transmitted power, bit-rate, cell size, FEC) could be easily evaluated and measured.

The complete implementation of such a system is under way, under the framework of the IRWLAN project.

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