Electronic Circuits for Wireless Optical LANs - I

Rui L. Aguiar, António Tavares, José Luis Cura, Eduardo de Vasconcelos,
Luis Nero Alves, Rui Valadas, Dinis M. Santos

***Resumo* – Este é o primeiro de dois artigos que discutem a implementação de emissores/receptores para redes locais não cabladas utilizando a tecnologia de infravermelhos, de baixo custo. O trabalho aqui apresentado cobre maioritariamente os elementos da camada física.**

As redes locais não cabladas consideradas têm taxas de transmissão entre 4Mbps e 25Mbps, e a capacidade do fotodíodo receptor entre 10pF e 50pF. Os tipos de modulação considerados são tipicamente 4-PPM ou 16-PPM.

Neste artigo são apresentadas diferentes topologias de front-end, quer em implementações discretas, quer em integradas (CMOS), tendo como objectivo diferentes redes alvo. Estratégias para melhoramento de largura de banda, redução de interferência, e melhoramento de gama dinâmica foram usadas em algumas destas topologias. Estas estratégias conduziram a um receptor de ganhos comutados com produto ganho*largura de banda de 25THzΩ , conseguidos com 10pF de capacidade do fotodíodo.

***Abstract* - This is the first of two papers discussing practical issues and results on the implementation of low-cost transceivers for several wireless optical LANs, covering most physical layer elements.**

Target optical LANs under consideration have bit-rates varying between 4Mbps and 25Mbps, and input photodiode capacitance may vary between 10pF and 50pF. PPM modulation, either in a 4-PPM or 16-PPM format, is typically used in the physical layer.

Several differential front-end topologies are presented both in discrete and integrated (CMOS) implementations, targeting different LANs. Strategies for bandwidth improvement, interference reduction and dynamic range improvement have been used in some of these topologies. These strategies lead to a switched-gain transceiver with a transimpedance gain*bandwidth of 25THzΩ , achieved with a 10pF capacitance photodiode.

Acronyms

A/D - Analogue-Digital
ADC - Analogue-Digital Converter
AGC - Automatic Gain Control (amplifier)
ASIC - Application Specific Integrated Circuit
AT - Adaptive Threshold
BER - Bit Error Rate
BW - BandWidth
CPLD - Complex Programmable Logic Device
CRC - Cyclic Redundancy Check
DPIM - Digital Pulse Interval Modulation
EMI - Electromagnetic Interference
FE - Front-End
FEC - Forward Error Correction
FOV- Field-Of-View
hpbw - half-power beam width
IR - Infra-Red
LAN - Local Area Network
LED - Light Emitting Diode
LNA - Low-noise Amplifier
MAP -Maximum A-Posteriori
MPDU - MAC Packet Data Unit
NRZ - Non-Return to Zero
PD - Photodiode
PLL - Phase-Locked Loop
PPM - Pulse Position Modulation
SNR - Signal to Noise Ratio
VGA - Variable Gain Amplifier
VCO - Voltage Controlled Oscillator
WLAN - Wireless Local Area Network
Z*BW - "transimpedance gain"*bandwidth

I. INTRODUCTION

Wireless optical communication systems have gone through considerable developments in recent years, as optical components have suffered important technologic advances and substantial price decreases. Thus data communications are increasingly using wireless optical systems at higher speeds. These systems are being used as an alternative to cabled media, mainly due to their simpler deployment and reconfiguration.

In wireless optical networks, major hindrance results from the low signal amplitudes that have to be used due to cost, health and power consumption constraints. Furthermore, the non-uniform nature of both the ambient noise and the signal power distribution puts increased demands on the dynamic range of the transceiver circuits. These wireless optical constrains call for new solutions, namely: (i) networks optimized for the usage of low cost optical components, (ii) development of systems with very flexible characteristics of gain and dynamic range, (iii) noise reduction techniques, and (iv) selection of optimal detector structures.

We have been developing wireless optical LAN systems pursuing these objectives. This paper documents some of our efforts in implementing practical low-cost transceivers. It is the first of two papers on the subject and thus comprises in Section II the target WLAN characteristics we used as reference for our work and the system reference block we have followed over the last years. Section III discusses some of the emitter characteristics, including the LED radiation diagram used. Section IV discusses front-ends that we have implemented; both in discrete and integrated format. The conclusions, in Section V, are brief, and are enlarged at the end of the companion paper.

The companion second paper addresses the sectorization problem, the MAP versus adaptive threshold detection and clock recovery issues. Considerations on overall practical apects are also presented, trying to highlight some problems in designing circuits for wireless LANs. Our conclusions, mostly as directions for future work, are presented in this second paper.
Note also that an independent paper on Signal-Noise measurements, also being presented in this issue, is of relevance to this work.

Most of the circuit blocks reported here have already been tested in various generations of working prototypes (with varying specifications). More recent work is currently under field test to assess its performance. Nevertheless, our current activity is focused on cooperative usage of these different circuit blocks, in order to provide efficient WLAN communications.

II. THE TARGET LAN(S)

A. Network Specifications

Our prototype WLANs have gone through several sets of specifications. Nevertheless we have always centered our efforts on diffuse (or multi-spot diffuse) packet networks. Packet format and size have been modified, as successive networks were refined. Cell size, transmitted power and bit-rate were the unstable parameters, as technology developments allowed for better and improved performance networks.
The work here described was developed for systems with varying specifications, with bit-rates between 1Mpbs and 25Mbps. Typical cells sizes are around 7×5×3m, and could face either natural or artificial illumination. Modulation methods varied from Differential Manchester to PPM. PPM modulation is frequently used in WLAN systems. It encodes words of N bits of information into one (and one only) active slot pulse inside a symbol with $M = 2^N$ time slots. This is known as PPM-N, where N is the order of the PPM modulation. Thus in PPM modulation, three different timing concepts exist: the slot duration, the bit duration, and the symbol (or word) duration. If T is the slot duration, then the unencoded bit lasts for N.T , and a symbol M.T. We used both 4-PPM and 16-PPM in our systems.
The target PD for these systems presents a relatively large junction capacitance, between 8 and 15pF, depending on the operating point. (Our current typical PD has an area of $0.07cm^2$ and a junction capacitance of about 12pF at the usual operation point). For increased sensitivity, photodiodes arrays have to be used. Typical systems used 5 to 15 PDs. These PDs have been selected in function of its low cost for a not extremely large junction capacitance. Although diffuse configurations were targeted, the non-uniformity in power distributions created by obstacles still demands for high dynamic range front-ends, able to operate with these low cost PDs.

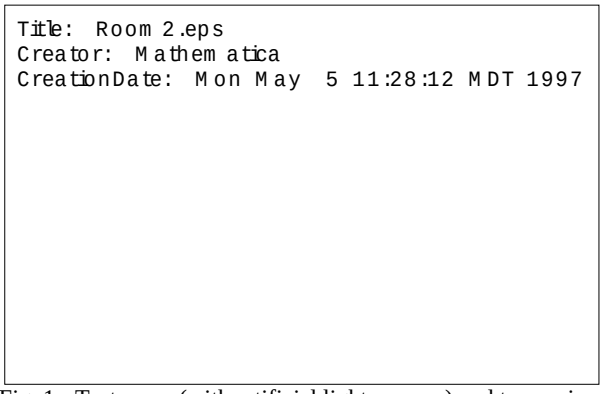

Fig. 1 - Test room (with artificial light sources) and transceiver model (sectored receiver represented).

The packet format used has a structure as shown in Table 1 [9], where Sync is the Synchronization field, SFD the Start Frame Delimiter, DR the Data Rate (signalizes the modulation/bit rate being transmitted) and DCLA is the DC Level Adjustment field. (This field is required due to the possibly different DC levels of the packet header and the rest of the packet, which being capacitively couple would cause DC level changes downstream). Length is the packet length, CRC the header check, and MPDU is the data packet, with variable size (but limited at most to 4500 bytes).
The specific packet format has been changed over the years. For instance, an EFD (End of Frame Delimiter) has also been used, the CRC field has not been always present, the maximum packet size has been changed, etc… These variations are, however, of minor consequence to the design of the electronic circuits supporting the WLAN, and we will neglect them across this paper.

B. Reference System

The basic network assumptions have been stable enough over the last few years for a basic structure to emerge from our implementations, regardless of varying network specifications and improvements in transducer technology. Our reference system is depicted in Fig. 1. It comprises an emitter, a receiver (eventually sectored), and the optical noisy indoor communication channel (a room with artificial lighting).
In this reference model, both the network protocol and the network transceiver are designed in order to achieve an efficient communication system with low complexity and low cost. As technology evolves, the point of equilibrium of these factors has changed, increasing the total

Table 1 - Frame format

Sync	SFD	DR	DCLA	Length	CRC	MPDU
57-73 slots	*4 slots*	*3 slots*	*32 slots*	*16 bits*	*16 bits*	*Variable*

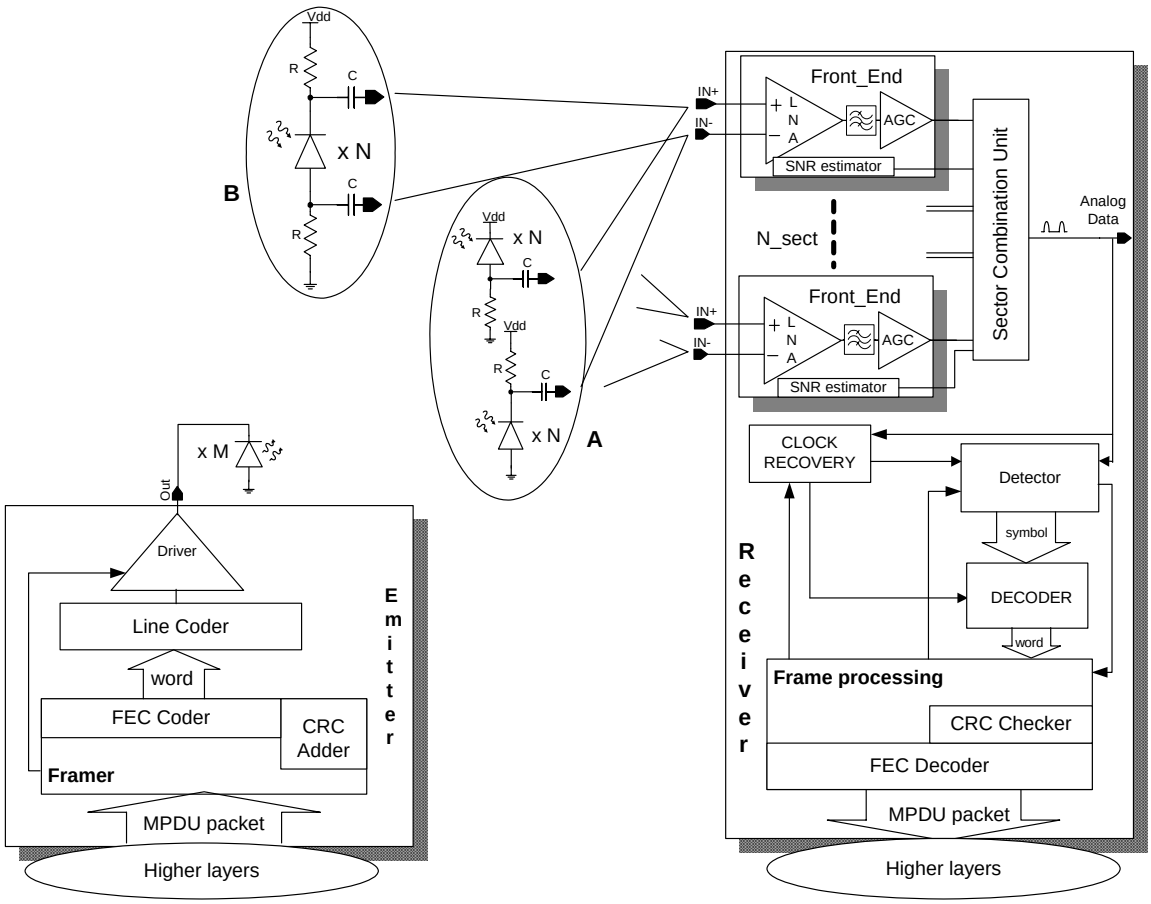

Fig. 2 - System block diagram.

bandwidth and the cell size while simultaneously reducing power consumption and transceiver size.

Fig. 2 presents the generic system block diagram of these transceivers. The following functions can be identified in the different communication entities:

Emitter:

a) Line driver — the unit responsible for the drive of the LED array.
b) Line coding/scrambling — the application of a proper line code chosen for performance, simplicity or power efficiency reasons; additionally the usage of a scrambler may be useful for certain non-limited run-length codes. We have used NRZ (plus scrambling), Differential Manchester and PPM (both 4-PPM and 16-PPM) in different systems.
c) FEC coding — the usage of FEC can improve the BER performance.
d) Framing operations — the usage of a packet-based network requires this block. It includes the wrap-up of the data with a preamble (and eventually a trailer), and the introduction of an (eventual) CRC field. The packet format has evolved over the years, as discussed in the previous section. We currently adhere to an IEEE 802.11-like format, as illustrated before.
e) System interface — the interface with the remainder of the sender system.

Receiver:

a) Front-end processing — this includes low-noise amplification, the usual current-to-voltage conversion, and an AGC, in order to achieve an analogue signal able to be post-processed. It may also include a filter, in order to improve noise performance. For high performance integrated front-ends, the filter is usually included in the front-end design.
b) SNR estimation — estimates the optical signal-to-noise ratio at the front-end. This estimation may be used either to control the AGC amplifier of the front-end for further combination (in Maximal-Ratio Receivers) or as a signal for the diversity combination unit (in Best Sector Receivers).
c) Sector combination — if several front-ends are used, some form of combination/selection of the different signals is required. This unit will output the "received" analogue signal. If SNR-dependent AGCs are used in the front-end, then some of the functions assigned to this unit may be performed there first. We have used both diversity and non-diversity configurations in our systems.
d) Clock recovery — a clock signal is required for digital detection. This clock is recovered from the analogue received signal. A fast lock on input signal is required.
e) Word detection — the detection of the received word. Three main strategies can be applied: threshold-

decision, adaptive threshold decision, and MAP detection. We tried all three strategies.

f) Word decoding/descrambling - upon detection of the line code word, word decoding will reconstruct the original information.
g) Un-framing -— all "packet" information has to be treated (this may imply control signals for the rest of the receiver units), and eventually a CRC check may have to be performed.
h) FEC decoding -— if FEC is used in the link, then a proper decoder has to be used (such as a Viterbi decoder).
i) System interface — the interface with the rest of the system.

In all these blocks dynamic power control can be applied, to decrease power consumption.

In the emitter, the MPDU goes through a unit responsible for frame formatting through the introduction of the several frame fields, including (possible) CRC generation. FEC coding may be applied afterwards, to improve transmission BER. This information is thus applied to a line coder, which converts information words to code symbols, and will finally attack a LED driver.

In the receiver, (possibly several) front-end(s) are driven by low-cost photodiodes. Two types of input connections are possible (see Fig. 2): case A, where different PDs are connected to each FE input; and case B, where the PDs are connected between both FE inputs. If diversity configurations are used, the signals received by these front-ends are delivered to a Selector Combination Unit. This unit will use some sort of SNR estimate per input signal to merge the individual outputs into a single analogue received signal [9,18]. This signal is delivered to a clock recovery unit (for clock recovery and line code alignment) and to a word detector. A decoder handles this signal, converting the received symbols in information words. Finally this information is passed to the frame-processing unit. This unit performs packet processing (removing all extra fields from the received packet, plus eventual CRC checking and FEC decoding) to finally achieve the transmitted information packet.

This structure allows some possible variants, as has been apparent from the above description. Network complexity (and performance) has increased with successive refinements of these layers. For instance, FEC can be used, but is not essential in the communication system, as some of our preliminary systems showed. Similarly, the usage of diversity receivers (requiring a SNR estimation and a selection combining unit) is not compulsory for achieving a working network, although it improves its efficiency in presence of non-uniform noise.

Therefore, the following sections detailing some of the blocks we have designed should not be interpreted as describing a single system. We aim to report on the practical feasibility and relative advantages of several transceiver sub-blocks, if used in a single system. We have used (and some times abandoned, in different degrees of its development) most of these structures and our current aim is the selection of the proper blocks for the implementation of a simple, compact and cost-efficient WLAN.

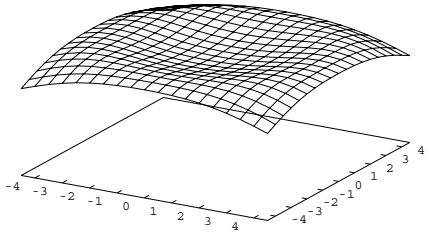

Fig. 3 - Power distribution on reference room.

For simplicity, we will omit the “system interface” units in the next sections. However, these may be quite complex, especially if the network uses a DPIM based system [6]. In DPIM, the relationship between the effective packet size and the number of bits transmitted is not constant, but data-dependent. As a consequence, frequency adaptation (both in the emitter and in the receiver) is required. Therefore, the system requires buffering and off-line processing, instead of real-time, clock dependent processing based in the clock relationships, as shown in [1].

III. EMITTER

A. Diffuse LED Head

We have designed and used for several years a diffuse radiation configuration [16]. This configuration was optimized in order to equalize the optical power distribution over the communication cell. In such optimization procedure, a square room with 9×9m and with a ceiling height of 3m was considered. The emitter radiation pattern was optimized with a simulation package reported in [11]. Simulations considered off-the-shelf low-cost LEDs and assumed up to sixteen LEDs. The simulations considered only the first order reflections on the room ceiling, which is a worst-case simulation. In real environments higher order reflections will increase the collected power, despite they may also decrease the power distribution uniformity.

The end result of the optimization procedure is presented in Fig. 3. With the configuration obtained through the optimization simulation package, the minimum value of the irradiance within the communication cell was about 57% of the maximum value achieved. Note that the presence of obstacles may change this power distribution substantially, and thus high dynamic range devices are still required even for this system.

The optical emitter was composed by two types of LEDs with the following characteristics: i) P_t = 12mW@50mA and hpbw = 15°; ii) P_t = 15mW@50mA and hpbw = 50°.

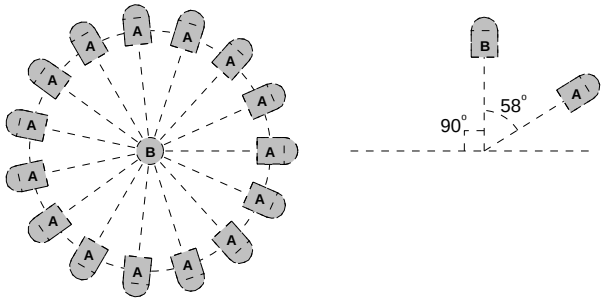

Fig. 4 - IR LED's horizontal distribution (left) and vertical orientation (right).

The LEDs were separated in two arrays with the following distribution and orientation (Fig. 4):

- 15 LEDs, type A, oriented at 58° with the vertical and uniformly distributed on the azimuth plane;
- 1 LED, type B, oriented vertically.

A simplified circuit of the optical emitter is presented in Fig. 5. The infrared LEDs were split in two branches of eight LEDs driven by two N-Channel MOSFET transistors. The IR driver emits an average optical power of about 400mW with a center wavelength of 850nm. Average current is about 105mA in each branch corresponding to a peak current of about 400mA. In order to improve switching times a pre-equalization technique is performed through the utilization of resistor R_2 and capacitor C_1.

The experimental results achieved with this driver have been quite satisfactory and proven to produce a remarkable diffuse radiation pattern in the rooms we usually use for test, even with the presence of normal obstacles (furniture, laboratory equipment, etc…)

B. Digital Processing

The implementation of the digital processing at the emitter can be divided in three aspects: line coding (usually trivial), the framing of the information (which we have initially done in an ASIC [1], although now current CPLD technology suffices for the bit-rates we are discussing) and FEC coding. A programmable convolutional coder, with a variable number of generator sequences and

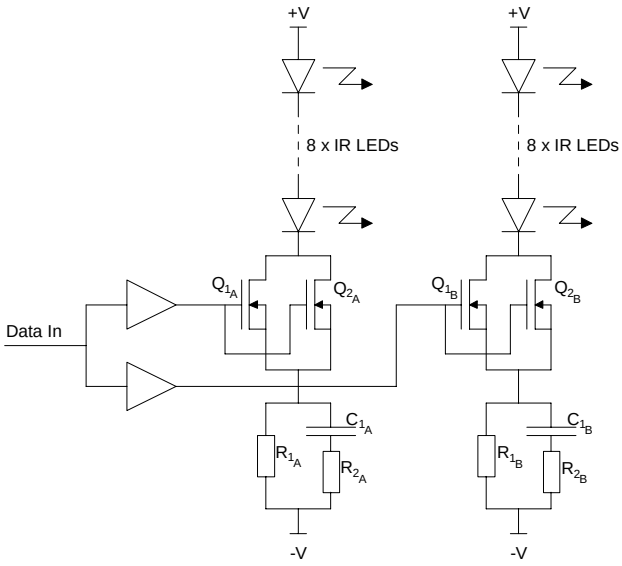

Fig. 5 - Optical emitter simplified circuit.

variable size has been recently implemented in a small size CPLD. Experimental results of the BER improvements achievable by the usage of different codes are still pending.

IV. FRONT-ENDS

A critical element for WLAN performance is the input stage of the Low-Noise Amplifier.

For analyzing this input stage, a current source with a capacitor in parallel can be used to model the input photodiode. Bias elements will then appear in parallel with the PD model. These elements impact system performance, as they create a band-pass filter at the input of the system.

Fig. 6 shows a typical model for the front-end input, including a simple LNA input model. In this figure, R_P is the bias resistor for the PD, R_{PD} and C_{PD} are the PD resistance and capacitance, R_{IN} and C_{IN} are the front-end input resistance and capacitance (the FE input impedance can be modeled in first approximation by these elements), and C_{acop} is the coupling capacitance. R_P has to be chosen according to the PD being used and the operating point

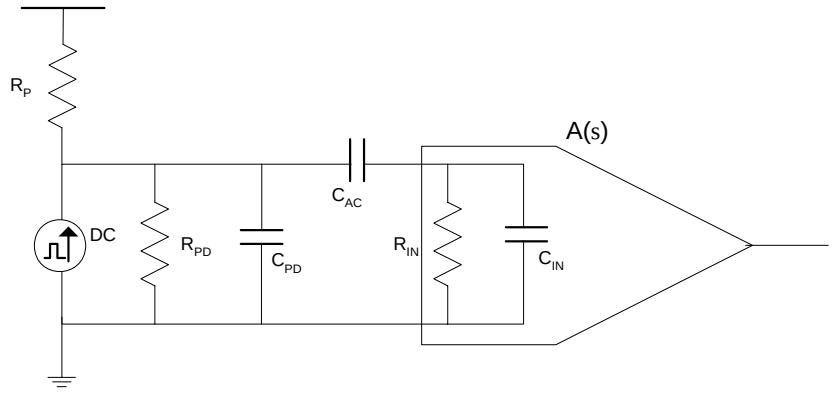

Fig. 6 - Simplified front-end input model.

desired.

The transfer function of this system, in terms of input current to the FE, is given by eq. 1. If we neglect the amplifier contribution to the transfer function, the input passive network presents a transfer function with two poles and one zero at the origin: a band-pass filter function, with a low (f_L) and high (f_H) cut-off frequencies. Note that the low cut-off frequency may be important for flicker noise reduction.

$$\frac{V_{out}}{I_{In}} = \frac{C_{AC}}{C_T} \frac{s}{s^2 + s\left(\frac{C_{AC}+C_{PD}}{C_T R_{IN}} + \frac{C_{acop}+C_{IN}}{C_T R_{//}}\right) + \frac{1}{C_T R_{IN} R_{//}}} A_V(s) \qquad (1)$$

$A_V(s)$ is the amplifier voltage gain, C_T is $C_{AC}C_{IN}+C_{IN}C_{PD}+C_{AC}C_{PD}$ and R// equals the parallel of R_P and R_{PD}

This expression can be used [2] to discuss the relative merits of the three key types of front-end topologies: high-impedance, low-impedance and transimpedance. Transimpedance amplifiers present the transimpedance amplifier; eq. 1 predicts the existence of a high-frequency pole dependent on the input capacitance. This is usually the dominant pole in WLANs front-ends best design trade-off for WLANs, and are thus the most commonly used. Note that even for a transimpedance amplifier, eq. 1 predicts the existence of a high-frequency pole dependent on the input capacitance. This is usually the dominant pole in WLANs front-ends.

A. Discrete Implementation(s)

A simplified block diagram of a discrete IR receiver is shown in Fig. 7, using the configuration B (Fig. 2). We have developed and published several discrete receivers ranging from 1Mbps to 4Mbps assuming Manchester line coding [16] and PPM modulation schemes [Valadas96].

An infrared optical receiver must have the highest possible sensitivity to reduce the required optical power (or in alternative to increase cell size). However, high sensitivity front-ends are very susceptible to EMI, which makes the design of the receiver quite a complex issue. To overcome the induced EMI, the receiver was designed with two complementary transimpedance amplifiers. This approach has two effective objectives: i) to use differential circuits in order to reduce the penalty induced by EMI; ii) to increase receiver bandwidth, for the same collected signal, avoiding equalization. To improve EMI immunity, the layout of the printed circuit board is carefully designed, with the complementary front-ends similarly implemented.

The IR receiver here referenced includes a photodiode array composed by five PIN photodiodes with a global active area of 0.35cm^2. Each photodiode has a junction capacitance of about 12pF. The measured gain of the complementary transimpedance amplifiers was about 154kΩ. Fig. 8 [9,10] shows the transimpedance gain for each one of the complementary front-ends. The measured bandwidth was about 7MHz, which is large enough for the requirements of a 4Mbps, 4-PPM network (the irregular response below 10kHz is due to measurement system artifacts). Following each complementary front-end there is a low-pass filter, and these signals were subtracted through a differential amplifier. The measured transimpedance gain of the complete receiver was about 1.2MΩ.

B. Integrated CMOS Front-Ends

We have then developed high-performance monolithic front-ends with two technological constraints:

i) target technology should be CMOS, due to its low cost and capabilities of very high integration; and

ii) the circuit should be designed to work with these low-cost photodiodes.

These constraints have a direct impact on front-end bandwidth. According to eq. 1, the input PD capacitance

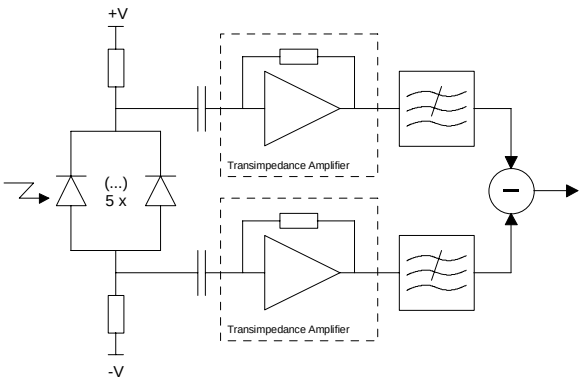

Fig. 7 - Block model of discrete IR front-end.

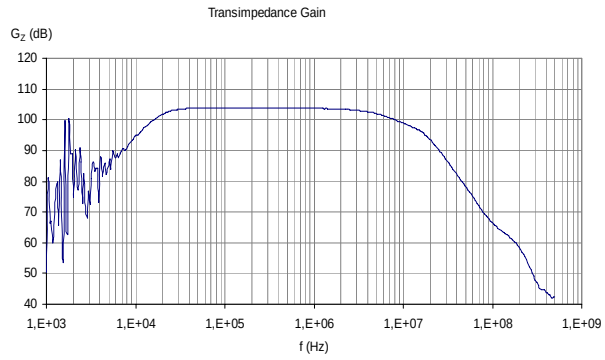

Fig. 8 - Measured transimpedance gain of a discrete low-cost front-end.

will limit the maximum front-end bandwidth (although possible, pole compensation is complex in these systems, due to the varying value of the input PD capacitance), and CMOS technology places limits on the maximum achievable transconductance gain per device. In practice, both factors imply that a (almost) dominant pole will appear in the circuit, created by the input impedance of the front-end and the parasitic PD capacitance.

We developed several integrated font-ends for baud rates raging from 2Mbps to 50Mbps, assuming both Manchester and 16-PPM modulation (DC levels in these codes are quite different). These front-ends were designed for input photodiodes with junction capacitance ranging from 10pF (for the higher bit rates) to 50pF. Besides the cut-off frequency imposed by the PD, the intrinsic bandwidth for these front-ends could be controlled externally. Thus we will limit the following discussion to the higher bit-rates, assuming input PDs with junction capacitance of ~10pF. Our design target was once more configuration B (Fig. 2) with the PD placed between both front-end inputs, due to its physical implementation advantages.
High dynamic ranges and low noise were sought for in all designs. These characteristics are required to cope with signal variations (reflection effects, single path illumination or the presence of obstacles can create large signal variations, even when using our "diffuse" configuration) and to optimize cell size. Furthermore signal filtering was done internally in all front-ends.

A single-ended input configuration with a switched gain approach [4] achieved a 10MHz BW, 48dB[1] dynamic range and 36pA/√Hz noise (see also Fig. 10). This circuit was rapidly evolved into two differential input configurations, in order to avoid electromagnetic interference, but was nevertheless useful for proving the switched gain concept: the large dynamic range possible in WLANs could be handled through a front-end which effectively changed its gain through (internal) discrete steps. This creates a simple structure that can be further optimized if smaller dynamic ranges are possible (achieved through better signal "diffusion", e.g.)

In [3], a 56MHz BW, 120kΩ gain differential front-end was implemented. Due to noise considerations, the LNA input has an input stage with a large NMOS [13], ideally matching the PD capacitance. The differential nature of the front-end would lead to a traditional differential first-stage. Unfortunately, for low-noise design and using the available technology, that approach does not achieve as large a bandwidth as desirable. Thus, a differential structure was implemented after an initial first stage with two independent LNAs, using starved inverters [Steyaert96]. A resistor, implemented with complementary switches, is used as the feedback element.

[1] We use logarithm units as 10log(A/B) throughout this paper, unless otherwise stated, due to the relationship between optical power and signal current on the PDs.

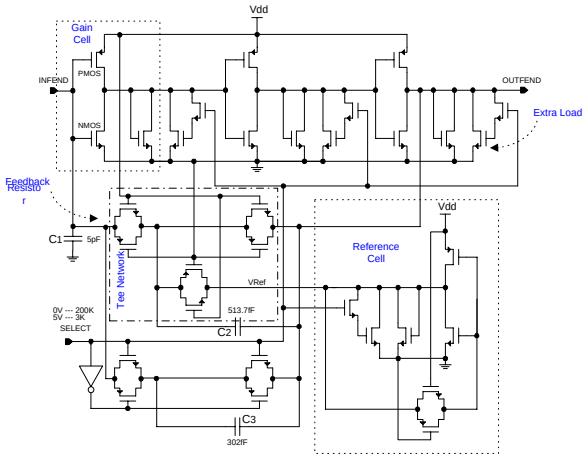

Fig. 9 - Loaded inverter single-ended amplification cell.

This resistor is designed using a T-configuration to decrease parasitic capacitance [7]. Nevertheless, stability considerations require individual compensation of the basic amplifier cell, dependent on the feedback resistor. In this circuit, stability issues are quite complex, as overcompensation would reduce bandwidth, and under compensation would lead to oscillations or large noise. The final result was a mixed compensation network, with a first-pole at the input, but with compensation along the feedback resistors also.
This front-end also implements a switched gain approach, changing the feedback resistors of the LNA to modify the transimpedance gain. The feedback resistor is switched depending on the input signal, in such a way that the system does not reach saturation. Furthermore, the switching system presents hysteresis in order to avoid gain oscillations.
The front-end further comprises a control stage, able to switch the gain from 3kΩ to 200kΩ and an automatic gain control (AGC) stage (with gain raging from 1 to 50). The LNA resolves input signals between ~20nA and ~100μA, with corresponding outputs ranging from 0.3V to 1.2V. The transimpedance amplifier cell is represented in Fig. 9, where the above mentioned blocks are clearly identified. The figure also shows a reference cell, used for setting the DC level of the feedback T-network.
As in the discrete case already discussed, two such amplification cells are then connected in a differential configuration, in order to produce a pseudo-differential amplifier.
This circuit was produced in a 5V, 0.8μm, double poly-, n-well CMOS technology. The front-end die size is 1200μm×600μm. Power consumption is 60mW.
This circuit has proven to be capable of large transimpedance gains, but requires careful compensation along the whole amplification loop.

In [19], we presented a differential structure, using initially low-gain transimpedance blocks, and then post-amplifying the output signal. This structure led to a 400kΩ, 55MHz BW front-end. The input signals can

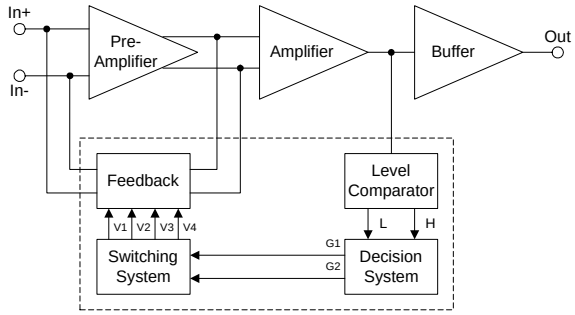

Fig. 10 - Block diagram of a switched gain differential front-end.

present values between 100nA and 100μA, duty-cycle independent. Output voltage ranges are from 40mV to 800mV.

The implemented circuit comprises three stages: a differential transimpedance amplifier with a switched feedback network, a differential to single-ended voltage amplifier and an output buffer, as shown in Fig. 10. The three stages are DC coupled to avoid baseline shift with signal input. Additionally a control block is added for gain switching purposes.

The topology used for the transimpedance amplifier is a modified folded cascode configuration [5,8] where the combination of two branches creates a differential stage, as shown in Fig. 11. For noise minimization considerations the transimpedance amplifier also presents an input stage with a large capacitance [13], once again ideally matched with the PD junction capacitance. Input referred current noise was under 8.2pA/√Hz. The input transimpedance amplifier was implemented with a step gain switched feedback network, achieving a 60dB dynamic range.

The RC series network at both input nodes is added for stabilization at the highest gain. The dimensions of the MOS transistor are such that the circuit's input resistance

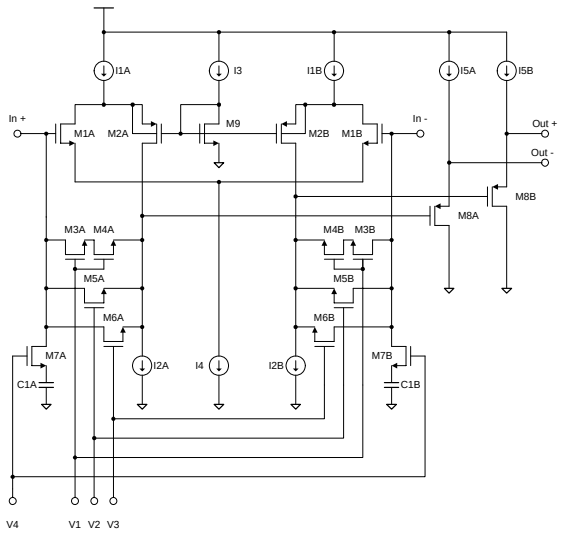

Fig. 11 - Folded cascode differential amplifier cell.

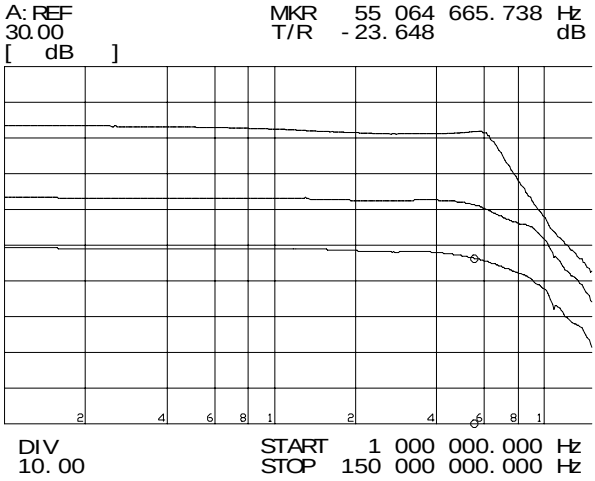

Fig. 12 - Measured transimpedance gains in the folded cascode front-end.

is low (of the order of 100Ω) when the circuit works at the highest gain. The RC network creates modified open-loop input impedance together with the input capacitance, allowing for pole-zero cancellation. The MOS transistor resistance value is increased to the order of hundreds of kΩ at lower gains, producing a negligible effect in the transfer function of the amplification stage.

This topology has been seen to be less noisy than the previous circuit, and also not so critically dependent on the compensation parameters. Nevertheless, it is quite sensitive to the DC operating point. If reduced specifications are required (smaller gain and/or bandwidth), both topologies, namely the folded cascode and the starved inverters configurations, can be used without such critical design considerations.

The differential to single-ended voltage amplifier that follows the input amplifier has a gain of approximately 9. The CMRR value, going from 100dB to 55dB over the entire bandwidth, is high enough to keep electromagnetic interference sufficiently low for the target application.

Fig. 12 shows measured results of the three transimpedance gains, with a 10pF junction capacitance PD across the input of the front-end. The compensation network effect controls the (here minimal) overshoot in the frequency response of the large gain.

This circuit was produced in a 5V, 0.8μm, double poly, n-well CMOS technology. The die size is 1600×1600μm (including pads). Power consumption is 60mW, of which more than 50% are due to the output buffers.

Fig. 13 confronts these approaches with other design choices. It represents several monolithic CMOS front-ends reported in the literature. Both the front-end bandwidth and the product of its transimpedance gain*bandwidth (Z*BW) are represented in a graph. The Z*BW factor is an easily calculated measure of the quality of the front-end. Note that (with the exception of [12], which has a large power consumption) values around ~20THzΩ seem to be the state-of-the-art current value, if large dynamic ranges are sought.

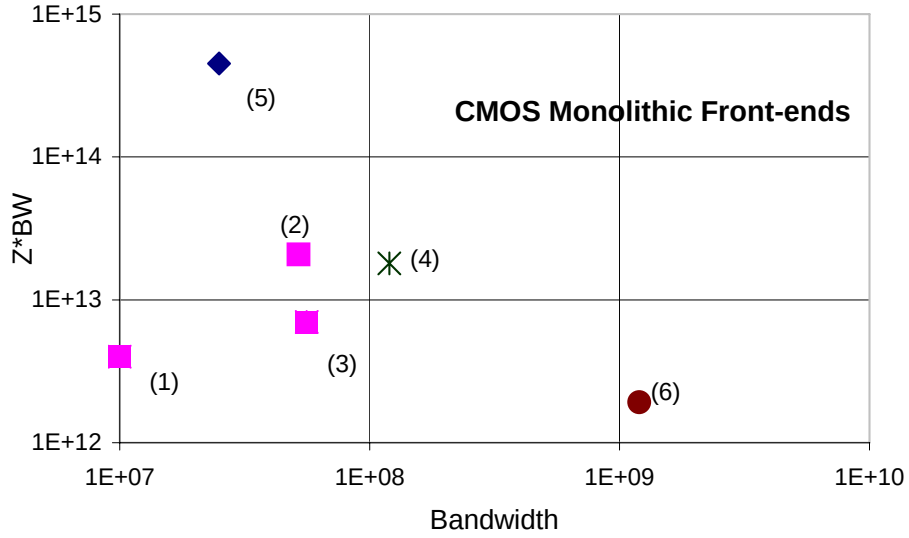

Fig. 13 - Gain*Bandwidth product versus Bandwidth for several monolithic CMOS front-ends.

Front-ends (1-4) were implemented in 0.8µm technologies. Only (1-2) have differential inputs. (1): [Carreiró99], (2): [19], (3): [Cura98], (4): [14], (5): [Pietruszynski88], (6): [17].

Values for (1-3) were measured with a 10pF input photodiode capacitance. (5) is measured with a 3pF input capacitance. (6) had a 0.25pF input capacitance. The input capacitance is not reported for (4).

Some of the values represented (in particular for (5)) were estimated. No linearity behaviour is known for (5).

Neither noise nor dynamic range are represented in Fig. 13, but both can be controlled if high enough Z*BW factors are possible in a given topology. Dynamic ranges of 25-40dB and noise levels of ~10pA/√Hz are reported in several papers. Z*BW values of near 20THzΩ seem to be achievable with present low-cost CMOS technologies, as we have proved.

These values may provide a practical rule-of-thumb for WLANs trade-off in terms of achievable bit-rate (for a given BER), cell size and emitter power.

VI. CONCLUSIONS

During this document we showed some key blocks for the implementation of wireless IR transceivers can be done with low-cost electronics, and still achieve high-performance results. The blocks here presented support the implementation of a diffuse WLAN, for bit-rates until 25Mbps, and with front-ends with gain*bandwidth product in the 20THzΩ range, with noise below 10pA/√Hz, for typical input PD junciton characteristics.

The companion paper will expand these conclusions for the overall WLAN network characteristics we are seeking to implement.

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The work here summarized is the result of several years of development in the field of low-cost WLAN transceivers, where implementation has always tried to follow network evolutions. Many elements have been involved with this work during these years, but a special mention should be done to Adriano Moreira and Cipriano Lomba, in the network aspects, and to Armindo Carreiró, Carla Almeida, Luis Moreira and Rui Antunes, in the implementation questions.

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