Groups of Synchronizers in Digital Communications

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Resumo - Neste artigo abordamos três importantes grupos de sincronizadores, nomeadamente o de fase, o de símbolo e o de bloco. Contudo dedicamos aqui a nossa atenção aos sincronizadores de símbolo onde distinguimos três grandes classes: a de malha aberta, malha mista e malha fechada.

Os sincronizadores de símbolo têm por objectivo amostrar os dados na máxima abertura do seu diagrama de olho, para retemporizar a duração dos bits com a mínima taxa de erros.

São vários os factores que desoptimizam o ponto de amostragem, mas destacamos o erro de fase estático (desajuste) e o erro de fase aleatório (jitter).

Os sincronizadores de simbolo podem ainda ser analisados pela sua gama de sincronismo e pela sua gama de captura.

Palavras chave: Sincronismo em Comunicações Digitais

Abstract - In this paper we deal with three important groups of synchronizers, namely the phase one, the symbol one and the block one. However here we dedicate our attention to the symbol synchronizers where we distinguish three big classes: the open loop, the mixed loop and the closed loop ones.

The symbol synchronizers have by objective to sample the data in the maximum opening of its eye diagram, to retiming the bits duration with the minimum bit error rate.

There are several factors that lead to a non-optimum sampling point, but we detach the static error phase (misadjust) and the random error phase (jitter).

The symbol synchronizers still can be analyzed by its lock range and capture range.

Key words: Synchronism in Digital Communications

I. INTRODUCTION

In data communication systems the signal must be transmitted and received, in analog systems with the minimum distortion and in digital systems with the minimum bit error rate.

A periodic signal is characterized by its amplitude and frequency (f=1/T), however when this signal is transmitted its amplitude varies with the distance emitter-receiver and its frequency varies with the relative speed emitter-receiver.

Then the analog systems which are sensible to the amplitude must possess an AGC (Automatic Gain Control) circuit that adjusts its gain maintaining an optimized output (ex. 1v) with minimum distortion and the digital systems must possess an AFC (Automatic Frequency Control) circuit that adjusts its frequency maintaining an optimized sampling (ex. $\Delta\phi=0$) with minimum bit error rate and correct retiming.

The effect of the AGC is attached to the linear part (front-end) and the AFC effect is attached to the non linear part (synchronizer), therefore the last one will be analyzed here.

In this work we study the open loop synchronizer (without AFC), the mixed loop synchronizer (with partial AFC) and the closed loop synchronizer (with total AFC).

We will analyze the 3 classes of synchronizers, in terms of static error phase (misadjust) with the input frequency variation (similar to the effect of mistuned components), in terms of synchronism / capture range and still in terms of random error phase (jitter) with the noise (SNR) [1].

Fig.1 shows the block diagram of a general synchronizer.

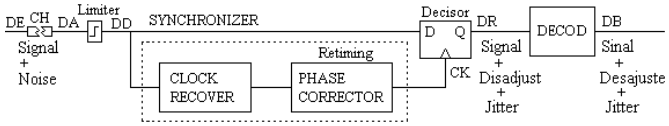

Fig.1 Block diagram of a general synchronizer

Some closed loop synchronizers have the phase corrector and the decisor circuit inlayed in the proper clock recover.

Fig.2 shows qualitatively as the static error phase (misadjusting) and the random error phase (jitter) increases the bit error rate.

The waveforms correspond to the points marked in the circuit. So DE is the data at the emitter, DA the analog data at the receiver input, DD the data with digital format, CK the recovered clock, DR the regenerated data at the synchronizer output and TE the error rate. DB is the data block.

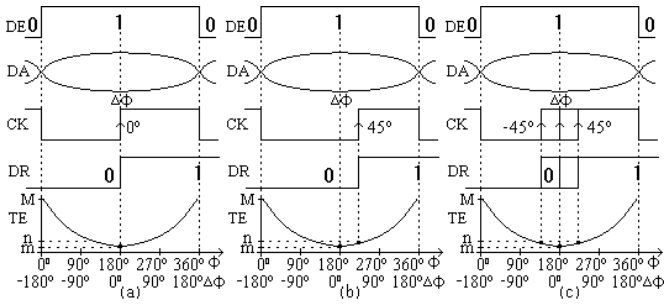

Fig.1 The clock samples the input signal

In Fig.1a there isn't misadjusting nor jitter, then the sampling occurs in the maximum opening of the eye diagram and the error probability is always minimum, in Fig.1b the misadjusting of 45º increases the error rate and in Fig.1c the jitter provokes random increasing of the error rate. If we have present the two error phases (static and random) the total effect aggravates the error probability, which varies with the random error phase $\Delta\phi$ between [0º, 90º].

If the synchronizer is out of synchronism, the error phase varies uncontrolled between [-180º, 180º] and the effect will be catastrophic with the error probability to shoot up.

II. SYMBOL SYNCHRONIZERS

A. Open Loop Synchronizer

The open loop synchronizer will be here represented by the tank circuit but could be any other open loop circuit as the case of the SAW (Surface Acoustic Wave) circuit or the digital circuits (monostable or astable) [2, 3, 4, 5].

Fig.3 represents the circuit tank, which is driven by data impulses at multiple intervals of the period.

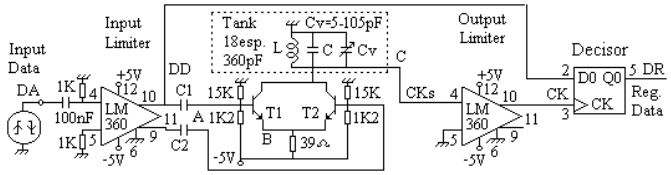

Fig.3 Open loop synchronizer (tank)

The 2 transistors in parallel operate in alternation one on the positive transitions and the other on the negative ones.

Fig.4 illustrates the functioning mode of the open loop synchronizer based in the circuit tank.

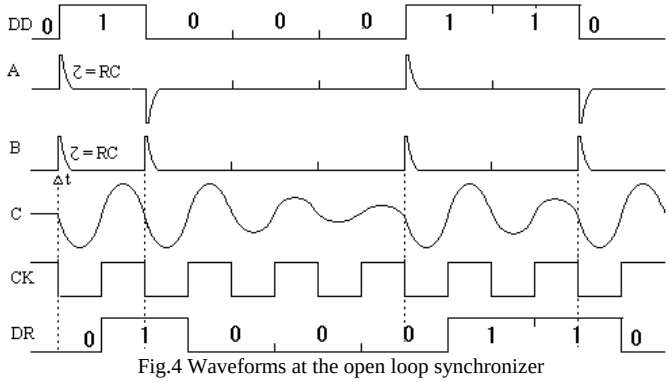

Fig.4 Waveforms at the open loop synchronizer

The input limiter gives digital format to the received signal. The differentiator concentrates the signal energy in the transitions at multiple intervals of the period that carries with itself a strong spectral line that after is selected by the high Q broadband filter. Then the comparator output catches this damped sinusoidal signal and convert it to a rectangular signal which is the recovered clock.

This circuit due to its simplicity allows high transmission rates but however the clock is of limited quality.

B. Mixed Loop Synchronizer

The mixed loop synchronizer shown in Fig.5 uses a conventional PLL after the open loop circuit, with intention to improve the features of the clock [6].

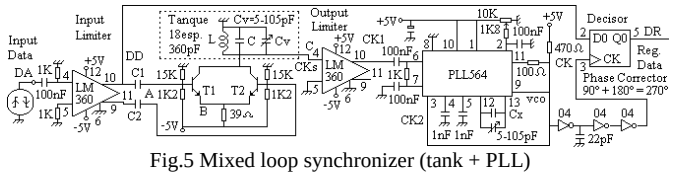

Fig.5 Mixed loop synchronizer (tank + PLL)

The mixed loop synchronizer is evidenced by an open loop circuit followed of a closed loop circuit.

Fig.6 shows the waveforms that illustrate the functioning mode of the mixed loop synchronizer.

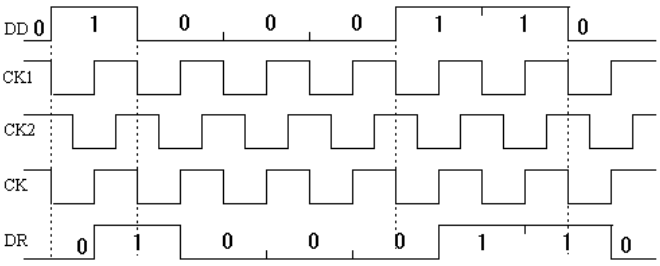

Fig.6 Waveforms at the mixed loop synchronizer

The operation of this circuit can be understood in 2 distinct parts, in the first one an open loop circuit (tank) produces a clock of lesser quality, in the second one a closed loop circuit (PLL) accept this input and provides an output version of good quality.

This synchronizer leaves out of the loop a considerable part of the total circuit, because only gets to synchronize its VCO with a signal which has a similar deterministic harmonic.

C. Closed Loop Synchronizer

The closed loop synchronizer can synchronize directly its VCO with the input random data and then all the components are inside of the loop [7].

Fig.7 shows the closed loop synchronizer where the VCO triggers the flip flop that samples the input data.

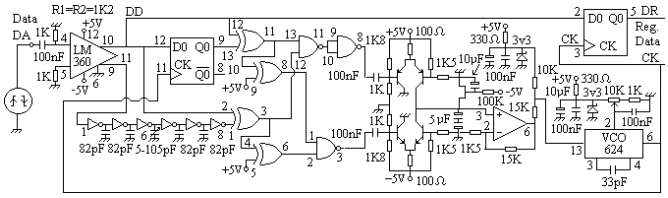

Fig.7 Closed loop synchronizer (triggered by VCO)

Fig.8 shows the waveforms that illustrate the functioning mode of the closed loop synchronizer.

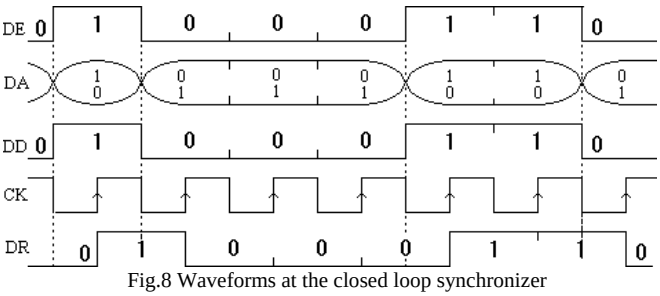

Fig.8 Waveforms at the closed loop synchronizer

The operation of this circuit is based on the comparison of a variable pulse against another fixed of reference (T/2).

When a data transition occurs initiates a variable pulse that finishes in the next positive transition of clock so that, the sampling (positive transition of the clock) occurs in the bit center. The duration of the variable pulse must be also equal to half period (T/2). Then the present synchronizer is a control system that acts on the positive transition of the clock

placing it in the center of the bit, that is, where generates a variable pulse equal to the fixed one produced between two consecutive transitions of the clock.

III. DESIGN, TESTS AND RESULTS

A. Test setup

To study the 3 mentioned synchronizers, we established three different comparisons, the first one at level of static error phase (misadjusting), the second one at level of synchronism / capture range and the third one at level of random error phase (jitter).

Fig.9 shows the general test setup, which allow to obtain the experimental and simulation results [10].

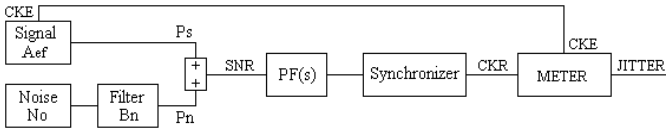

Fig.9 Block diagram of the test setup

The two first comparisons was made experimentally using the oscilloscope as the real measure device. The third comparison was made experimentally with the measure device (ANDO), but some difficulties in controlling the noise in a "GAP", obliged us later to resort to the simulation.

For this reason, we created the equivalent simulation models of the real circuits and after we used a powerful mathematical tool to make the processing.

The design and dimensioning of the circuits were made by form to provide equal conditions and can be meet in [8].

The prefilter was not used in this work (PF(s)=1), but can be useful for high noise quantities [9].

B. Results at level of static error phase

Fig.10 shows the experimental results obtained with an oscilloscope, for the 3 classes of synchronizers, when the input varies its transmission rate (frequency).

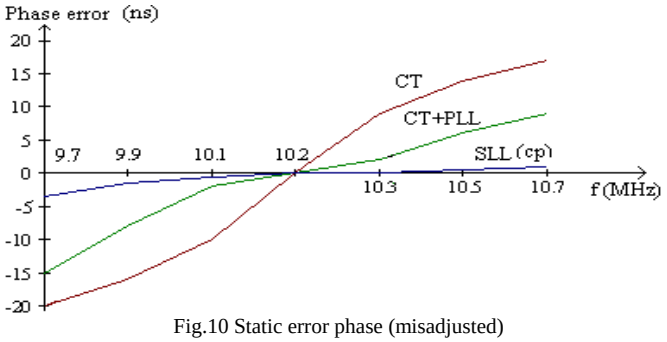

Fig.10 Static error phase (misadjusted)

Identical results would be waited if we maintain the input, but on the other hand we mistuned the circuits.

We verify that the open loop synchronizer is the one that produces greater static error phase for the same variation of the input frequency. After, the mixed loop synchronizer begins to feel the effect of a partial closed loop diminishing the error phase. Finally, the closed loop synchronizer possess a total loop between the VCO and input, therefore any misadjusting is strongly reduced, by the loop, to a low value.

We must still point out, that the closed loop synchronizer can increment the loop gain, reducing the static error, however must be preserved the loop stability.

C. Results at level of synchronism / capture range

Fig.11 shows the results of the 3 classes of synchronizers at level of operation / synchronism range.

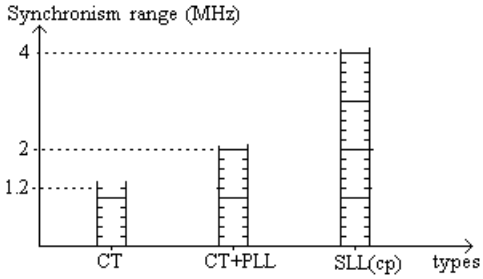

Fig.11 Operation / synchronism range

We verify that the closed loop synchronizer possess greater operation/synchronism range than the mixed one and this has a bigger range than the open loop one.

Fig.12 shows the results of the 3 classes of synchronizers at level of operation / capture range.

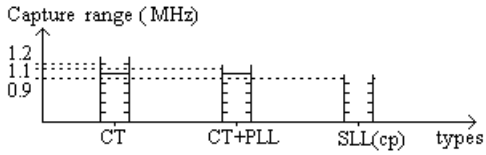

Fig.12 Operation / capture range

We verify that the closed loop synchronizer possess minor operation/capture range than the mixed one and this a lesser range than the open loop one.

D. Results at level of random error phase

Fig.13 shows the output jitter in UIRMS (Unit Intervals Root Mean Squared) as function of the input SNR (signal to noise relation) for the 3 cited synchronizers.

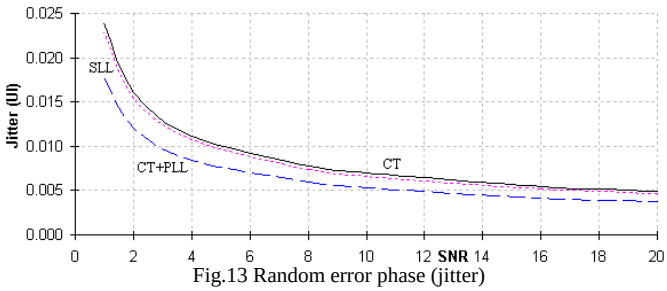

Fig.13 Random error phase (jitter)

We verify that the open and closed loop synchronizers have similar jitter performance but the mixed one has a slightly advantage due to its double tuning, especially for low SNR. For high SNR the 3 synchronizers tend to be identical.

These results were measured with parameters that provide identical linear operation modes for the 3 synchronizers.

The open and mixed loop synchronizers do not possess AFC total and this imposes that the filter broadband Bf be sufficiently large to avoid the risk to go out of tuning when the input varies.

On the other hand, the closed loop synchronizer possess AFC total and scanning circuit, then the VCO (extracted clock) nearly follows the input transmission rate, so a narrowband filter can be used what implies a reduced loop noise bandwidth Bl and consequently a lower jitter.

IV. ANOTHER CLOSED LOOP SYNCHRONIZER

A. Synchronizer triggered by input

The closed loop synchronizer that we shown previously was triggered by VCO (VCO acting the flip-flop clock) now we go to present another synchronizer but that is triggered by input (entered acting the flip-flop clock). Both closed loop synchronizers are sequential because they possess memory.

In Fig.14, the proposed synchronizer possesses auxiliary scanning circuit, which strongly increases the capture range to a value similar to the synchronism range.

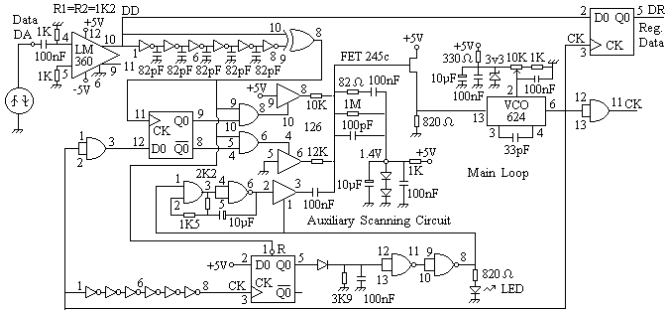

Fig.14 Closed loop synchronizer triggered by input

Tab.1 shows the effect of the scanning circuit

Tab.1 – Synchronism and capture ranges

SYNCHRONISM RANGE

Transmission rate (frequency MHz)	Phase error (ns)
11	+ 1
10.6	+ 0.25
10.2	+ 0+
10	0
9.8	− 0+
9.4	− 0.5
9	− 1.5
8.5	− 2.5
8	− 5

8 --- 10 --- 11
1M + 2M = 3 MHz
(a)

CAPTURE RANGE

Transmission rate (frequency MHz)	Phase error (ns)
10.2	+ 0+
10	0
9.8	− 0+

9.7 --- 10.2 --- 10.8
200 + 200 = 400 KHz
− --> Delayed clock
+ --> Advanced clock
(b)

CAPTURE RANGE WITH AID

Transmission rate (frequency MHz)	Phase error (ns)
11	+ 1
10.6	+ 0.25
10.2	+ 0+
10	0
9.8	− 0+
9.4	− 0.5
9	− 1.5
8.5	− 2.5
8	− 5

8 --- 10 --- 11
1M + 2M = 3 MHz
(c)

We verify that the capture range without aid is incremented, becoming similar to the synchronism one.

By this way the only possible disadvantage of the closed loop synchronizer is also favorably solved.

When the synchronism is restored, the synchronism detector, with luminous signaling, disactivates the scanning generator, leaving it in high impedance, for not disturbing the functionality of the main circuit.

B. Jitter-noise curves of the 2 closed synchronizers

Fig.15 shows the experimental curves of jitter-SNR (optical power variation) for the 2 closed loop synchronizers.

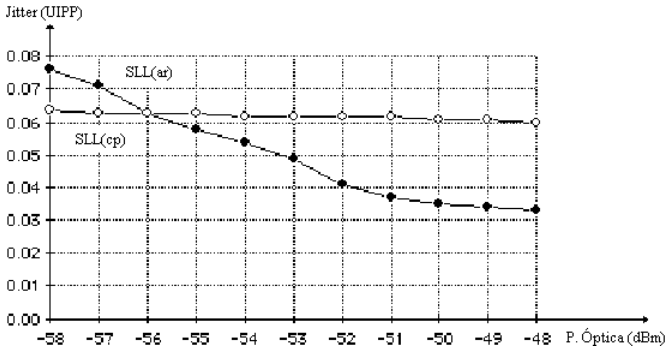

Fig.15 Output jitter as function of the input optical power

We verify that for low SNR (Ps<-56dBm) the triggered one by VCO gains advantage, but for high SNR (Ps>-56dBm) the triggered one by input presents some advantage.

Fig.16 shows the simulation curves of output jitter UIRMS as function of the input SNR for the 2 synchronizers.

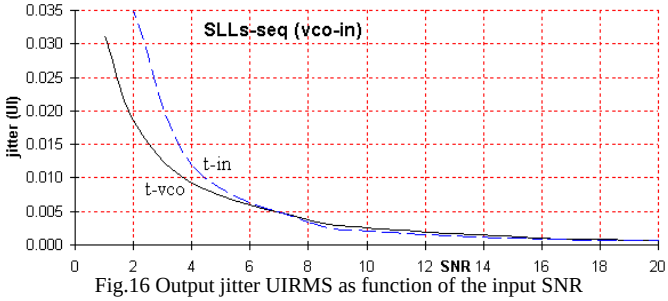

Fig.16 Output jitter UIRMS as function of the input SNR

We verify that for low signal noise relations (SNR<6) the triggered by VCO gains advantage, but for high signal to noise relation (SNR>6) is the triggered one by input that presents a slightly advantage.

The optical signal power Ps and the noise signal power Pn are related by the formula (SNR=Ps/Pn).

Generally we can say, such as in the experimental jitter-noise curves, also in the simulation ones we verified that for low SNR the synchronizer triggered by VCO gains some advantage, but for high SNR is the synchronizer triggered by input that gains a slightly advantage.

C. Output jitter versus input frequency jitter

We made other more experimental tests over the 2 closed loop synchronizers. The test now consisted to measure the output jitter amplitude, when it is injected an input signal with constant jitter amplitude (0.2 UIPP (Unit Interval Peak to Peak)) but with variable frequency.

Fig.17 shows the curves output jitter - input jitter when the entered keeps its amplitude (0.2 ÙIPP) but varies the frequency.

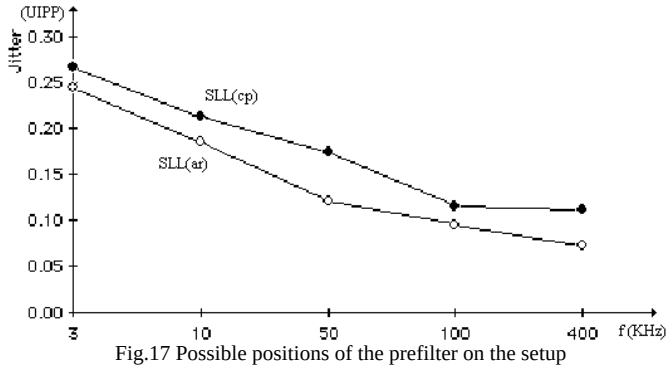

Fig.17 Possible positions of the prefilter on the setup

We verify that the output jitter amplitude diminishes, when the input jitter frequency increases, although one maintain its amplitude (0.2 UIPP).

V. CONCLUSIONS

We considered 3 classes of symbol synchronizers namely the open loop, the mixed loop and the closed loop, then we established comparisons at level of static error phase (misadjusting), at level of synchronism / capture range and at level of random error phase (jitter).

We verify that the closed loop synchronizer only can present some disadvantage in relation to the capture range but that can also be recouped with the aid of the slow scanning circuit.

The results show that the closed loop synchronizer guarantees the lesser static error phase (misadjusting) and consequently also the greater stabilization of its components. This synchronizer endowed with scanning circuit also possesses the best operation/synchronism/capture range.

For the same bandwidth of the filter Bf / loop noise bandwidth Bl, the 3 classes of synchronizers present similar curves of random error phase (jitter). However it must be mentioned that the closed loop one possess AFC and therefore the loop filter can be reduced without problems, with the consequent reduction of the loop noise bandwidth and logically also with the reduction of the jitter.

VI. ACKNOWLEDGMENTS

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