Systems of Synchronism in Digital Communications

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Resumo - **A transmissão fiel da informação à distância é um sonho primitivo do homem. Embora notemos uma grande evolução é ainda possível introduzir melhorias.**

O sinal transmitido sofre atenuação e distorção, então é necessário que periodicamente um regenerador reponha a energia perdida (amplificador com AGC) e retemporize o sinal com a mínima taxa de erros (sincronizador com AFC).

Palavras chave: **Sistemas de Sincronismo**

Abstract - **The faithful transmission of information at distance is a Man's primitive dream. Although we notice a great evolution it is still possible to introduce improvements.**

The transmitted signal suffers attenuation and distortion, then it is necessary that periodically a regenerator replaces the lost energy (amplifier with AGC) and retimes the signal with the minimum bit error rate (synchronizer with AFC).

Key words: Systems of Synchronism

I. INTRODUCTION

In this paper we ignore the part of the amplifier with AGC (Automatic Gain Control) and we center our attention in the part of the synchronizer with AFC (Automatic Frequency Control).

The final quality of a communication system depends in good part of the synchronizer, which makes an important function of bits duration retiming (Fig.1a) with minimum bit error rate (Fig.1b).

Fig.1a shows that the pulses, transmitted by the emitter, with duration T enlarge until the receiver and then is necessary to retime them newly. On the other hand Fig.1b evidences, in the emitter, the correct sampling and illustrates, in the receiver, as a null error phase of the clock relatively to the data minimizes the bit error rate.

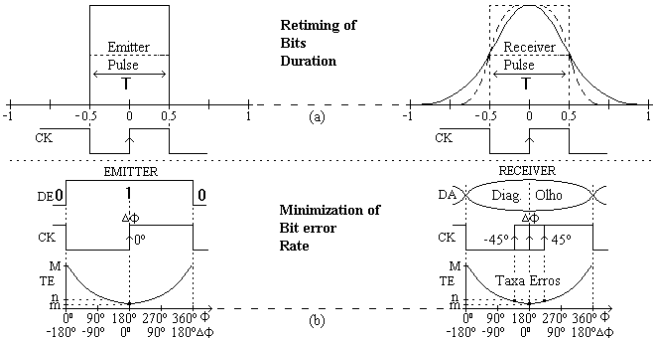

Fig.1 Retiming of bits (a) and correct sampling (b)

The main objective of this work consists in developing synchronizers of closed loop for high transmission rates. We research the possibility of the synchronizers operate internally at low frequency and transmit externally at high rhythms.

We begin introducing the synchronizer in a general data transmission system to analyze the involved problems, opting after by the more appropriate synchronizer.

We define three groups of synchronizers, namely the one of phase (SF), symbol (SS) and block (SB). However we consider only the symbol synchronizer, where we distinguish three classes, namely the one of open loop (ma), mixed loop (mm) and closed loop (mf).

In the closed loop symbol synchronizers, we distinguish four types, namely the analog (ana), the hybrid (hib), the combinational (cmb) and the sequential (seq).

We explore the sequential synchronizers potentialities operating at data subrates transmission. We develop prototypes operating at the proper data rate (tx1), at half data rate (tx2) and at a quarter data rate (tx4).

II. SYNCHRONIZER AS PART OF A SYSTEM

To better understand the function of the synchronizer, we go to introduce it in a general data transmission system (Fig.2). By this way, we stay with a global idea of the synchronizer function and only later we will stay preoccupied with its internal operation.

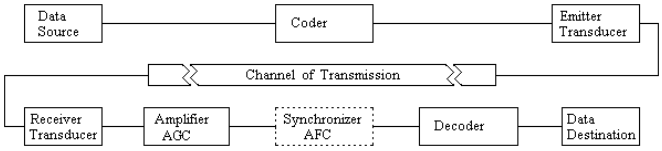

Fig.2 General system of data communication

In the simplified block diagram we have:
Emitter:
Data source (beginning of the data);
Coder (the data are coded with the appropriated form);
Transmitter transducer (the electric energy is converted in other energy form matched to the channel);
Receiver:
Receiver transducer (the transmitted energy is newly converted in electric energy);
Amplifier with AGC (the lost energy in the transmission is restored);
Synchronizer with AFC (retimes the duration of the bits with the minimum bit error rate);
Decoder (data are decoded for the original form);
Data destination (data are processed to the desired effect);

III. SYNCHRONIZER

The synchronizer can assume several tasks, thus we detach three groups, namely the phase synchronizer (SF), the symbol synchronizer (SS) and the block synchronizer (SB). The phase synchronizer theory is quite important because it is also valid for the symbol and block synchronizers. However in this work we concentrate our attention on the symbol synchronizer.

A. Symbol synchronizer

In the symbol synchronizers of Fig.3, we distinguish three great classes, namely the one of open loop (ma), the one of mixed loop (mm) and the one of closed loop (mf) [1, 2, 4].

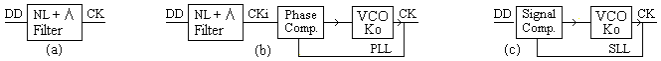

Fig.3 Open loop (ma), mixed (mm) and closed (mf)

In the open loop symbol synchronizer all its blocks are outside of the loop, in the mixed loop there are some blocks outside but others are already inside the loop and in the closed loop all the blocks are inside of the loop.
The comparison between these various classes of synchronizers can be very useful in the course of research to take place in the future.

IV. CLOSED LOOP SYMBOL SYNCHRONIZERS

In the symbol synchronizers of closed loop, we distinguish four great types, namely the analog, the hybrid, the combinational and the sequential. It is the type of signal comparator that determines the type of synchronizers, because the others blocks are equals. Thus if we use the analog signal comparator we will obtain the analog synchronizer and the same happen with the hybrid, combinational and sequential.
Fig.4 shows the closed loop symbol synchronizer of analog type (ana).

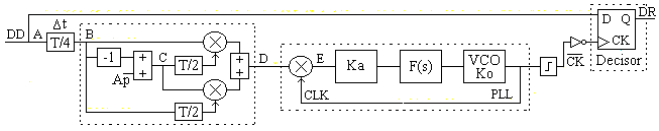

Fig.4 Closed synchronizer of analog type (ana)

We verify that all the components of the signal comparator are analog and there isn't limiter in the inputs (DD, VCO).
Fig.5 shows the closed loop symbol synchronizer of hybrid type (hib).

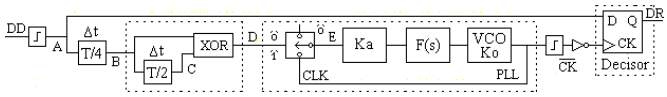

Fig.5 Closed synchronizer of hybrid type (hib)

We verify that the components of the signal comparator are hybrid (semi-analog or semi-digital) and there is a limiter only in the input DD.

Fig.6 shows the closed loop symbol synchronizer of combinational type (cmb).

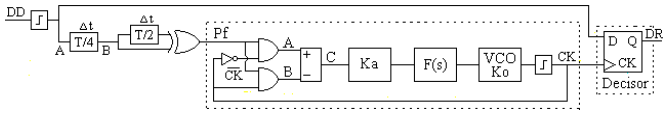

Fig.6 Closed synchronizer of combinational type (cmb)

We verify that all the components of the signal comparator are digital combinational (without memory) and there are limiters in both inputs (DD, VCO).
Fig.7 shows the closed loop symbol synchronizer of sequential type (seq).

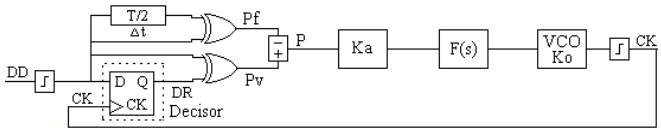

Fig.7 Closed synchronizer of sequential type (seq)

We verify that some components of the signal comparator are digital sequential (with memory) and there are limiters in both inputs (DD, VCO).

V. SEQUENTIAL SYNCHRONIZERS OF HIGH RATE

The sequential synchronizers possess a signal comparator with memory and therefore they have design potentialities that the others don't have. It is then easy to create automatic versions and topologies that operate at submultiples of the

transmission rate. This capacity, of the circuits operating internally at low frequency and transmitting externally at high rate, is important and will be illustrated following [6].

We begin presenting the prototype that operates at the proper data transmission rate and that will be used as base of beginning for the prototypes operating at subrates (Fig.8).

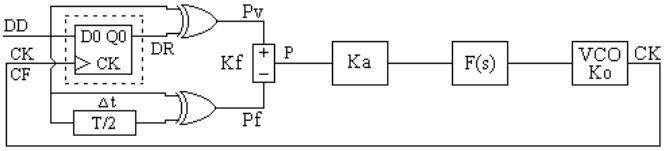

Fig.8 Sequential operating at proper rate (tx1)

The internal operation frequency is equal to the proper external data transmission rate.

In Fig.9 we present the prototype that operates at half of the data transmission rate.

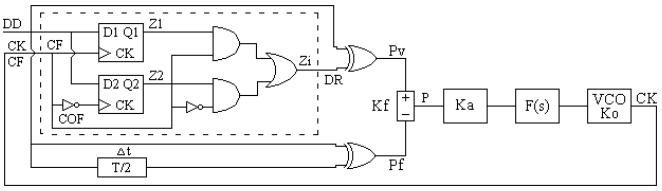

Fig.9 Sequential operating at half rate (tx2)

The internal operation frequency is only half of the external data transmission rate.

In Fig.10 we present the prototype that operates at a quarter of the data transmission rate.

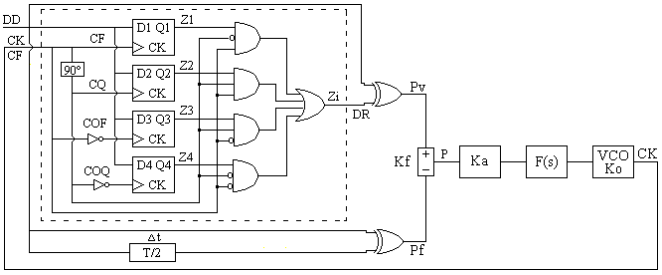

Fig.10 Sequential operating at quarter rate (tx4)

The internal operation frequency is only a quarter of the external data transmission rate.

This base idea of parallel processing can be generalized and then extended to topologies operating at $1/N=1/2^n$ of the data rate.

In Fig.11 we present the prototype that operates at one over N of the data transmission rate.

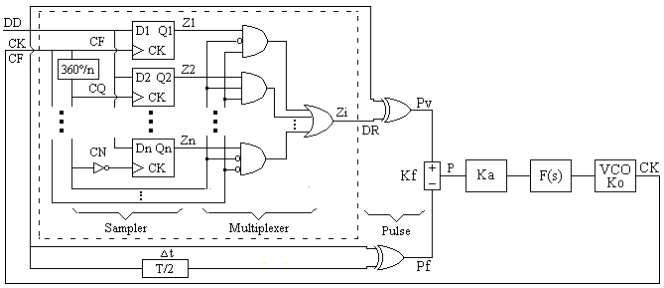

Fig.11 Sequential operating at one over N rate (txN)

The internal operation frequency is only one over N of the external data transmission rate.

VI. DESIGN, TESTS AND RESULTS

A. Test setup

Fig.12 shows the setup that we used to get the jitter-noise curves of each synchronizer [5].

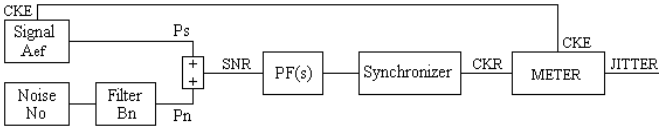

Fig.12 Block diagram of the test setup

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

Here, we did not used the prefilter (PF(s)=1), which can be useful when the noise is quite high [3].

B. Jitter measurer

Fig.13 shows the jitter measurer (METER), which consists in a RS flip flop, that detects the recovered clock phase variation (VCO) relatively to the fixed phase of the emitter clock. This relative phase is the jitter of the recovered clock.

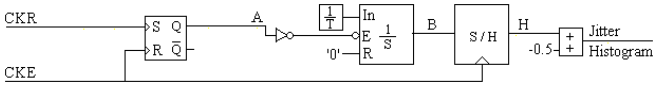

Fig.13 The jitter measurer device

The others blocks convert this phase variation into an amplitude variation which is the jitter histogram.

Fig.14 shows the waveforms that illustrate the operation mode of the jitter measurer.

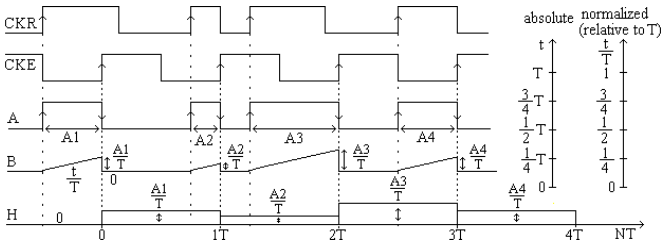

Fig.14 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving its average, jitter variance in squared radians, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

C. Loop parameters design

To perform comparisons, it is necessary to design all the loops with identical linearized transfer functions.

The loop gain is given by Kl=Kd.Ko=Ka.Kf.Ko where Kd is the phase detector gain, Ko is the VCO gain and Kf is the phase comparator gain. However, the amplification factor Ka is the control parameter that acts in the roots location to allow the desired characteristics.

To test the synchronizers, we used a normalized data rate tx=1 Baud, that simplifies the analysis, giving normalized values for the others parameters. Thus we used a clock frequency fCK =1Hz, an external noise bandwidth Bn=5Hz and a loop noise bandwidth Bl=0.02 Hz.

The output jitter UI is function of the input SNR (UI=f(SNR). The relation between SNR and σn is $SNR=Ps/Pn=Aef^2/No.Bn = Aef^2/(2\sigma n^2\,\Delta\tau\,Bn) = (0.5)^2/(2\sigma n^2*10^{-3}*5) = 25/\sigma n^2$.

Here we used only the 1st order loop with an insignificant filter F(s)=0.5Hz, however the 2nd order one is also useful.

-1st order loop

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st loop is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \qquad (1)$$

the loop noise bandwidth for the SLL (Symbol Lock Loop) is

$$Bl = \frac{KdKo}{4} = Ka\frac{KfKo}{4} = 0.02Hz \qquad (2)$$

thus for the analog and hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \text{ --> } Ka = 0.08\frac{2.2}{\pi} \qquad (3)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4} = Ka\frac{(1/\pi)2\pi}{4}=0.02Hz \text{ --> } Ka = 0.04 \quad (4)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4} = Ka\frac{(1/2\pi)2\pi}{4}=0.02Hz \text{ --> } Ka = 0.08 \quad (5)$$

The 2nd order loop is also used in many applications.

D. Results of the various synchronizers

Fig.15 shows the RMS jitter in units intervals UI, as function of the input signal to noise ratio SNR. It is considered the synchronizers (all analogs) of open loop (ma), mixed loop (mm) and closed loop (mf). It is considered the synchronizers of closed loop, namely the analog type (ana), hybrid (hib), combinational (cmb) and sequential (seq). It is still considered the sequential synchronizers (with memory) operating at the proper bit rate (tx1), at half rate (tx2) and at a quarter rate (tx4).

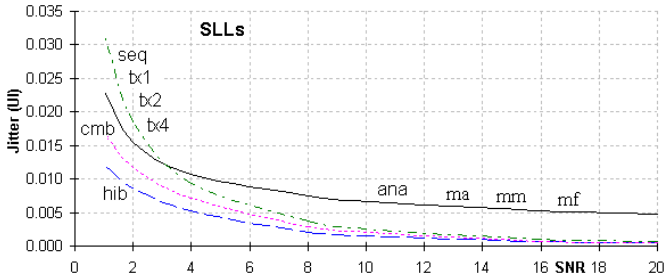

Fig.15 Jitter-noise for (ma, mm, mf, ana, hib, cmb, seq, tx1, tx2, tx4)

We verify that the analog synchronizers without limiter in the input (ma, mm, mf, ana) do not have noise margin.

The digital synchronizers, with limiter, are advantageous for high SNR due to its noise margin. However for low SNR the sequential one stay in disadvantage due to its memory which drives to the error state.

VII. CONCLUSIONS

We studied the symbol synchronizers of open loop (ma, mixed loop (mm) and closed loop (mf), we verify that being all them analog and with the same external bandwidth Bl, possess similar jitter-noise curves, although with a slightly advantage for the one of mixed loop, due to its duple tuning.

We studied the closed loop symbol synchronizer of analog type (ana), hybrid (hib), combinational (cmb) and sequential (seq). The analog one don't possess limiter in the input, while the others possess it, so with high SNR the noise margin effects gives advantage to the digital synchronizers. However for low SNR, the sequential synchronizer feels the effect of its memory, that drives to the error state aggravating the jitter. This disadvantage can be minimized with the prefilter. The combinational synchronizer, with digital components, has a similar performance to the hybrid and then it is a good

choose in terms of jitter, but the memory absence of its signal comparator limits the design potentialities.

We studied the sequential synchronizers based on pulses comparison and we verified that maintain its jitter-noise curve, although operates at different ratios of the transmission rate (tx1, tx2, tx4).

VIII. ACKNOWLEDGMENTS

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