Closed Loop Symbol Synchronizers

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Resumo - **Neste documento apresentamos quatro tipos de sincronizadores de malha fechada, nomeadamente o analógico, o híbrido, o combinacional e o sequencial.**

No sincronizador de fase a diferença entre os vários tipos estava dentro do comparador de fase, de modo semelhante nos sincronizadores de símbolo essa diferença está dentro do comparador de sinal.

O nosso objectivo principal é estudar o comportamento de jitter, dos vários sincronizadores, na presença do ruído e então estabelecer algumas comparações.

Abstract - **In this paper, we present four types of closed loop symbol synchronizers, namely the analog, the hybrid, the combinational and the sequential.**

In the phase synchronizers the difference between the various types was inside the phase comparator, with a similar mode in the symbol synchronizers this difference is inside the signal comparator.

Our main objective is to study the jitter behavior, of the various synchronizers, in the noise presence and then to establish some comparisons.

I. INTRODUCTION

In this work, we consider four types of closed loop symbol synchronizers that are the analog, the hybrid, the combinational and the sequential.

All synchronizers types recover the clock perfectly synchronized with the incoming data, in order to retime the output regenerated data with the minimum bit error rate

Although the various synchronizers perform the same function, its constitution differs from one to another. This difference is essentially located in the signal comparator, since the others blocks are similars.

Fig.1 illustrates the composition of the phase and symbol synchronizers.

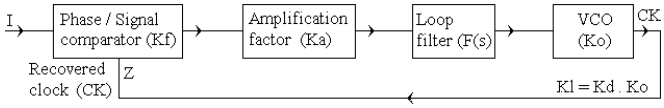

Fig.1 Block diagram of phase and symbol synchronizers

In the phase synchronizer surged the idea to distinguish four different types, namely the analog, the hybrid, the combinational and the sequential.

Although the phase lock loop (PLL) operate well with an input signal similar to the VCO, they have some difficult to synchronize directly with the input data. Thus we developed the equivalent symbol lock loop (SLL) which can synchronize directly with the input data.

The fundamental difference between the phase synchronizers and the symbol synchronizers is in the input comparison block (phase / signal comparator).

The phase comparator allow to implement the respective phase synchronizers whereas the signal comparators allow to implement the respective symbol synchronizers. Both phase and symbol synchronizers have four types, that are the analog, the hybrid, the combinational and the sequential.

$$\text{Phase / Symbol Synchronizers} \begin{cases} \text{Analog} \\ \text{Hybrid} \\ \text{Combinational} \\ \text{Sequential} \end{cases}$$

We will ignore the phase synchronizers and we will concentrate our attention only in the symbol synchronizers.

Afterwards, we will show the implementation of the four types of symbol synchronizers.

Next, we will present the test setup, design and results of the various synchronizers.

Finally, we will see the main conclusions.

II. PHASE AND SIGNAL COMPARATORS

The difference between the phase and the signal comparators is inside the comparator block. Thus we will show the phase and signal comparators in order to evidence its particular characteristics [1, 2, 8, 9].

A. Phase comparators

Fig.2 shows the four types of phase comparators, namely the analog (a), the hybrid (b), the combinational (c) and the sequential (d) [3, 6].

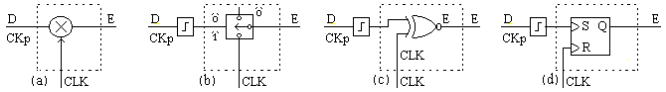

Fig.2 Phase comparators

The phase comparator works well with a periodic input signal that is similar with the VCO, but have some difficult to synchronize directly with a random input data.

B. Signal comparators

Fig.3 shows the four types of signal comparators, namely the analog (a), the hybrid (b), the combinational (c) and the sequential (d) [4].

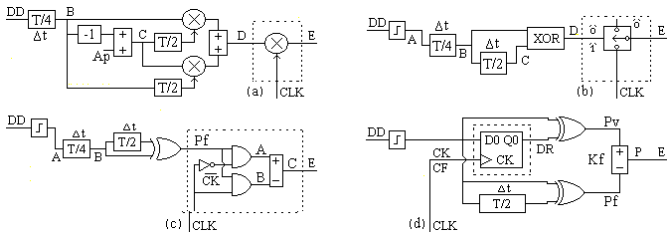

Fig.3 Signal comparators

The signal comparator has the capacity to synchronize directly with a random input data.

However, in this work, we will consider only the signal comparators, that implement the respectives symbol synchronizers.

III. CLOSED LOOP TOPOLOGIES

The four topologies of closed loop symbol synchronizers SLL (Symbol Lock Loop) are obtained introducing the signal comparators in a conventional PLL (Phase Lock Loop) [5].

A. Analog synchronizer

Fig.4 shows the analog closed loop synchronizer that is composed by the analog phase comparator, amplification factor, filter and VCO.

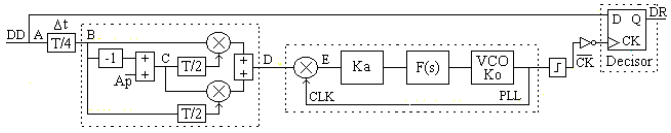

Fig.4 Analog closed loop synchronizer

The input signal of the SLL and the VCO output, at the phase comparator input, are both analog.

B. Hybrid synchronizer

Fig.5 shows the hybrid closed loop synchronizer that is composed by the hybrid phase comparator, amplification factor, filter and VCO.

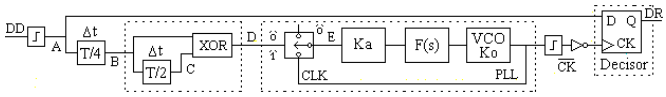

Fig.5 Hybrid closed loop synchronizer

The input signal of the SLL is digital but the VCO output is still analog.

C. Combinational synchronizer

Fig.6 shows the combinational closed loop synchronizer that is composed by the combinational phase comparator, amplification factor, filter and VCO.

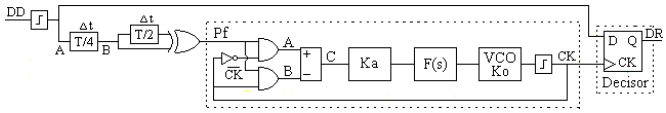

Fig.6 Combinational closed loop synchronizer

The two inputs of the phase comparator are both digital and its output is only function of the entries.

D. Sequential synchronizer

Fig.7 shows the sequential closed loop synchronizer that is composed by the sequential phase comparator, amplification factor, filter and VCO.

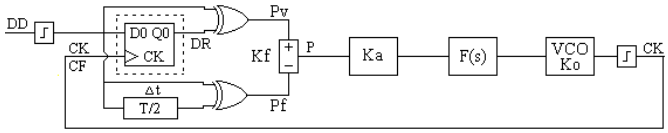

Fig.7 Sequential closed loop synchronizer

The two inputs of the phase comparator are both digital but now its output depends simultaneously on the two entries and also on the phase comparator state (memory).

IV. DESIGN, TESTS AND RESULTS

A. Test setup

Fig.8 shows the setup that we used to get the jitter-noise curves of the various synchronizers [7].

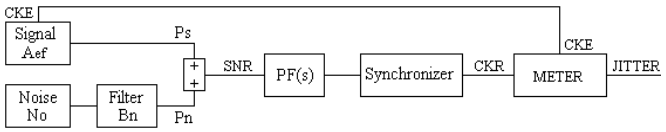

Fig.8 Block diagram of the test setup

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

The prefilter is not used here (PF(s)=1).

B. Jitter measurer

Fig.9 shows the jitter measurer (METTER) that consists of a RS flip-flop which detects the variable phase of the recovered clock (VCO) relatively to the fixed phase of the emitter clock.

This relative phase variation is the recovered clock jitter.

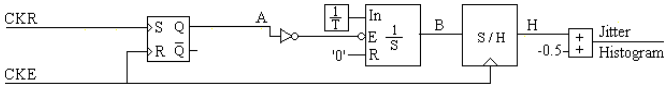

Fig.9 The jitter measurer device

The others blocks convert this phase variation into an amplitude variation which is the jitter histogram.

Fig.10 shows the waveforms that illustrate the operation mode of the jitter measurer.

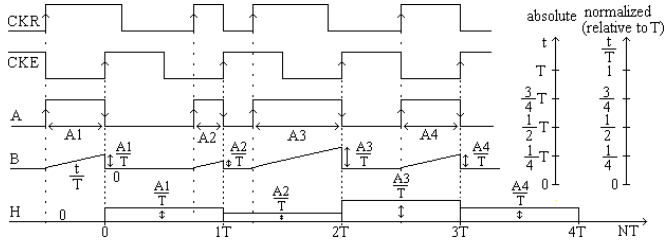

Fig.10 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving the average m, jitter variance in squared radians σ_n^2, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

We have used also others jitter measurers with similar results.

C. Loop parameters design

To establish guaranteed comparisons it is necessary to test all the synchronizers in equal conditions.

We use a normalized transmission rate tx=1 baud (fo=1Hz) what facilitates the analysis and allows one more easy extrapolation for other rhythms of transmission. We use an equivalent external noise bandwidth Bn=5Hz for all SLL. For the closed loop symbol synchronizers SLL we use a loop noise bandwidth Bl=0.02Hz.

For the analog SLL the relation between SNR and σn is $SNR=Aef^2/No.Bn=Aef^2/(2\sigma n^2.\Delta\tau.Bn)=(0.5)^2/(2\sigma n^2*10^{-3}*5)=25/\sigma n^2$. This relation is more complicated for the others symbol synchronizers.

We will now present the loop parameters design for the various PLLs considering the first (1st) and the second order loop (2nd).

- 1st order loop:

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st order is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth for the SLLs is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

so for the analog SLL with Km=1, A=1/2, B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \text{ --> } Ka=0.08\frac{2.2}{\pi} \quad (3)$$

for the hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \text{ --> } Ka=0.08\frac{2.2}{\pi} \quad (4)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/\pi)2\pi}{4}=0.02Hz \text{ --> } Ka=0.04 \quad (5)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/2\pi)2\pi}{4}=0.02Hz \text{ --> } Ka=0.08 \quad (6)$$

This formulas are useful in high speed circuits

- 2nd order loop:

The transfer function with $F(s)=\frac{1+sT2}{sT1}$ is

$$H(s)=\frac{sKdKo(T2/T1)+KdKo/T1}{s+sKdKo(T2/T1)+KdKo/T1} \quad (7)$$

$$=\frac{sA+B}{s^2+s2\xi Wn+Wn^2} \quad (8)$$

and the loop noise bandwidth is

$$Bl=\frac{\xi Wn}{2}\left(1+\frac{1}{4\xi^2}\right) \quad (9)$$

Taking (ξ=1 and Bl=0.02) and solving the above equations we obtain for F(s)

$$F(s) = \frac{1 + s63}{s977} \qquad (10)$$

so for the analog SLL we have

$$Kd=KaKf= Ka(1)(1/2)(1/2) = \frac{1}{2\pi} \text{ --> } Ka = \frac{2.2}{\pi} \qquad (11)$$

for the hybrid SLL we have

$$Kd=KaKf= Ka(1)(1/2)(0.45) = \frac{1}{2\pi} \text{ --> } Ka = \frac{2.2}{\pi} \qquad (12)$$

for the combinational SLL we have

$$Kd=KaKf=Ka\frac{1}{\pi} = \frac{1}{2\pi} \text{ --> } Ka = 0.5 \qquad (13)$$

and for the sequential SLL we have

$$Kd=KaKf=Ka\frac{1}{2\pi} = \frac{1}{2\pi} \text{ --> } Ka = 1 \qquad (14)$$

This formulas can be used in others synchronizers.

D. Results

We studied the behavior of the four closed loop symbol synchronizers in the presence of the noise.

Fig.11 shows the jitter-noise curves of the four closed loop symbol synchronizers, namely the analog SLL (ana), the hybrid SLL (hib), the combinational SLL (cmb) and the sequential SLL (seqv).

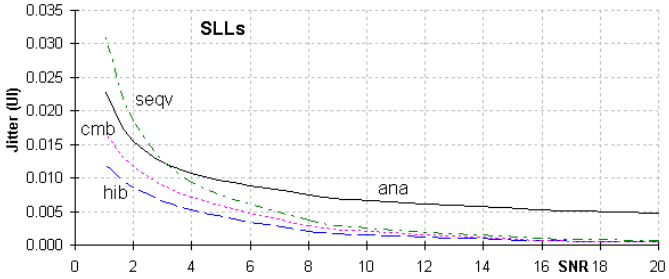

Fig.11 Jitter-noise curves of the four mixed topologies

We tested the various types of SLL with white noise that is summed to an input of digital signal format (rectangular).

We verify that for high SNR (SNR>4) the synchronizers with limiter in the input (hybrid, combinational and sequential) perform better than the synchronizer without limiter in the input (analog).

For low SNR (SNR<4), the sequential synchronizer (with memory) begins with synchronism problems and therefore performs worst than the others.

Apparently in terms of jitter, the hybrid and the combinational synchronizer have the advantages of the analog one for low SNR and the advantages of the sequential one for high SNR, however the sequential type has more design potentialities.

V. CONCLUSIONS

In this work we considered the phase and the signal comparators. In both we distinguish four types, namely the analog, hybrid, combinational and sequential. However we implemented and analyzed only the four symbol synchronizers corresponding to the signal comparators.

The results show that for high SNR (SNR>4) the synchronizers with limiter in the input (hybrid, combinational and sequential) present better jitter performance than the synchronizer without limiter in the input (analog). This is comprehensible since in the hybrid, combinational and sequential, the limiter is a digital component with noise margin in which low noise spikes are ignored, whereas in the analog synchronizer there isn't this limiter and therefore until the low noise is considered.

For low SNR, the noise spikes are greater than the component noise margin and then we must evaluate its effects on the jitter output. The sequential synchronizer has worst performance than the others. This is comprehensible since the sequential synchronizer is a system with states (memory) and when it processes the input in the error state the output jitter increases strongly. However this disadvantage of the sequential synchronizer can be minimized with the prefilter.

Apparently the hybrid and combinational synchronizers are the best option since they have a good performance for low and high SNR. However the sequential one is a circuit with memory which allows to design manual and automatic versions operating at the data and subdata transmission rates.

VI. ACKNOWLEDGMENTS

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