Effects of the Clock Transition Slope on the Symbol Synchronizers

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Resumo - **Neste artigo apresentamos quatro tipos de sincronizadores de malha fechada, nomeadamente o analógico, o híbrido, o combinacional e o sequencial.**

Também mostramos duas configurações de teste desses sincronizadores, uma com a inclinação da transição do relógio abrupta e outra em que há alguma redução da inclinação da transição.

O principal objectivo é estudar os efeitos da inclinação da transição do relógio sobre os quatro sincronizadores. Então mostraremos e compararemos as suas curvas de jitter-ruído.

Palavras chave: **Sincronismo em Comunicações Digitais**

Abstract - **In this paper we present four types of closed loop symbol synchronizers, namely the analog, the hybrid, the combinational and the sequential.**

Also we show two test configurations of these synchronizers, one with an abrupt clock transition slope and other with some clock transition slope reduction.

The main objective is to study the effects of the clock transition slope on the four synchronizers. Then we will show and compare its jitter-noise curves.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

In this work, we study four synchronizers that are the analog, the hybrid, the combinational and the sequential. The difference between these synchronizers is inside of the signal comparator, thus the others blocks are similar.

We consider two configurations for these synchronizers, in the first the clock is fed back without any clock transition inclination reduction and in the second the clock is fed back with some clock transition inclination reduction.

We intend to see as the clock transition inclination can affect the four synchronizers jitter behavior in the presence of noise.

Fig.1 shows the general aspect of the closed loop symbol synchronizer with direct clock feedback.

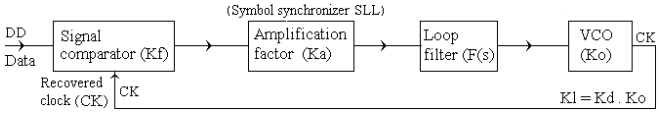

Fig.1 General closed loop symbol synchronizer (SLL)

In this configuration, the clock is fed back such it is provided by the VCO, without any transition inclination reduction.

After we will introduce a block that can make some transition inclination reduction.

Thus, we will present these two configurations that are the normal configuration and the reduced configuration.

Next, we present the four synchronizers (analog, hybrid, combinational, sequential) evidencing the reduction block.

Afterwards, we show the design, tests and results with some comparisons [1, 6, 7].

Finally, we present the main conclusions.

II. CONFIGURATIONS OF THE TRANSITION

Fig.2 shows the two configurations of the synchronizers, in the first one the clock of the four synchronizers is fed back without any transition inclination reduction (a) and in the second one the clock of the four synchronizers is fed back with some transition inclination reduction (b) [4].

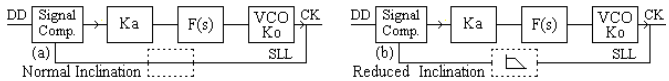

Fig.2 Normal configuration (a), reduced configuration (b)

The difference between these two configurations is in the block of clock transition inclination. We will study the two configurations of the four synchronizers with comparisons.

A. Without inclination reduction

In the configuration (a) the clock of the four synchronizers is fed back as it is generated by the VCO, without any transition inclination reduction.

B. With inclination reduction

In the configuration (b) the clock of the four synchronizers is fed back modifying the VCO slew rate, with some transition inclination reduction.

III. CLOSED LOOP TOPOLOGIES

We consider four symbol lock loop (SLL), named as the analog, hybrid, combinational and sequential [3].

A. Analog closed loop symbol synchronizer

Fig.3 shows the analog closed loop synchronizer that is composed by the analog signal comparator, amplification factor, filter and VCO.

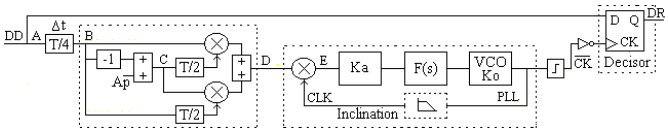

Fig.3 Analog symbol lock loop

The input signal of the SLL and the VCO output, at the signal comparator input, are both analog.

B. Hybrid closed loop symbol synchronizer

Fig.4 shows the hybrid closed loop synchronizer with the respective signal comparator and the others blocks.

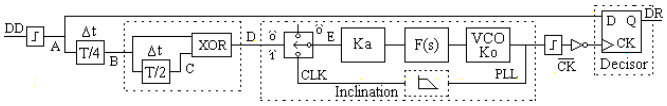

Fig.4 Hybrid symbol lock loop

The input signal of the SLL is digital but the VCO output is still analog.

C. Combinational closed loop symbol synchronizer

Fig.5 shows the combinational closed loop synchronizer with the respective signal comparator and others blocks.

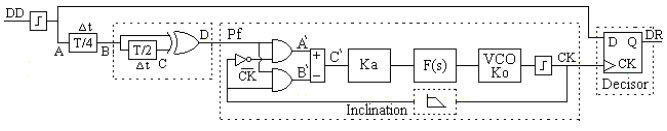

Fig.5 Combinational symbol lock loop

The two inputs of the signal comparator are both digital and its output is only function of the entries.

D. Sequential closed loop symbol synchronizer

Fig.6 shows the sequential closed loop synchronizer with the respective hybrid comparator and others blocks [2].

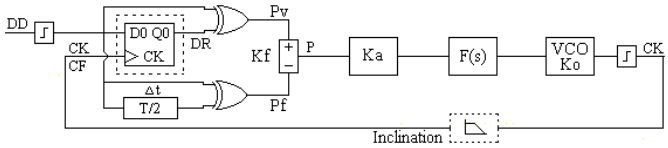

Fig.6 Sequential symbol lock loop

The two inputs of the signal comparator are both digital but now its output depends simultaneously on the two entries and also on the signal comparator state (memory).

IV. DESIGN, TESTS AND RESULTS

A. Test setup

Fig.7 shows the setup that we used to get the jitter-noise curves of the various synchronizers [5].

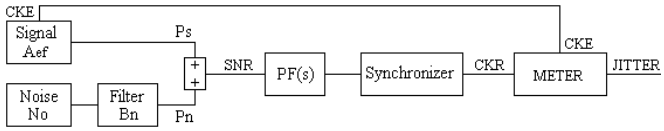

Fig.7 Block diagram of the test setup

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

The prefilter is not used here, but can be useful in system with high noise quantities (PF(s)=1).

B. Jitter measurer

Fig.8 shows the jitter measurer (METTER) that consists of a RS flip-flop, which detects the variable phase of the recovered clock (VCO) relatively to the fixed phase of the emitter clock.

This relative phase variation is the recovered clock jitter.

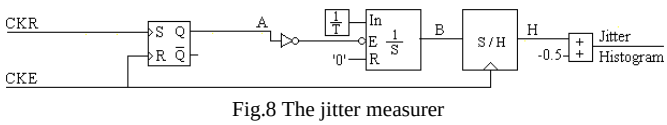

Fig.8 The jitter measurer

The others blocks convert this phase variation into an amplitude variation, which is the jitter histogram.

Fig.9 shows the waveforms that illustrate the operation mode of the jitter measurer.

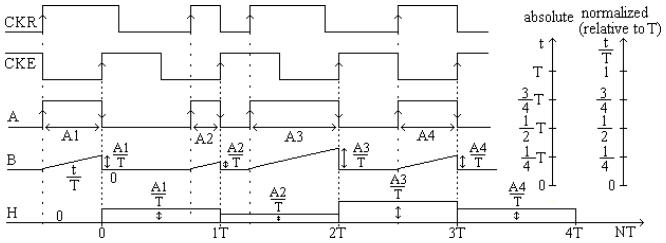

Fig.9 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving the average, jitter variance in squared radians σ_n^2, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

We have used also others jitter measurers with similar results.

C. Loop parameters design

To establish guaranteed comparisons it is necessary to test all the synchronizers in equal conditions.

We use a normalized transmission rate tx=1 baud (fo=1Hz) what facilitates the analyses and allows a easier extrapolation for other rhythms of transmission. We use an equivalent external noise bandwidth Bn=5Hz for all SLL. For the closed loop symbol synchronizers SLL, we use a loop noise bandwidth Bl=0.02Hz.

For the analog SLL, the relation between SNR and σn is $SNR=Aef^2/No.Bn=Aef^2/(2\sigma n^2.\Delta\tau.Bn)=(0.5)^2/(2\sigma n^2*10^{-3}*5)=25/\sigma n^2$. This relation is more complicated for the others symbol synchronizers.

We will now present the loop parameters design for the various PLLs considering the first (1st) and the second order loop (2nd).

- 1st order loop:

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st order is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \qquad (1)$$

the loop noise bandwidth for the SLLs is

$$B1=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \qquad (2)$$

so for the analog SLL with Km=1, A=1/2, B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz\Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (3)$$

for the hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02\Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (4)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/\pi)2\pi}{4}=0.02\Rightarrow Ka=0.04 \qquad (5)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/2\pi)2\pi}{4}=0.02\Rightarrow Ka=0.08 \qquad (6)$$

These formulas are useful in synchronizer design

- 2nd order loop:

The transfer function with $F(s)=\frac{1+sT2}{sT1}$ is

$$H(s)=\frac{sKdKo(T2/T1)+KdKo/T1}{s+sKdKo(T2/T1)+KdKo/T1} \qquad (7)$$

$$=\frac{sA+B}{s^2+s2\xi Wn+Wn^2} \qquad (8)$$

and the loop noise bandwidth is

$$B1=\frac{\xi Wn}{2}\left(1+\frac{1}{4\xi^2}\right) \qquad (9)$$

Taking (ξ=1 and Bl=0.02) and solving the above equations we obtain for F(s)

$$F(s)=\frac{1+s63}{s977} \qquad (10)$$

so for the analog SLL we have

$$Kd=KaKf$$
$$=Ka(1)(1/2)(1/2)(0.45)=\frac{1}{2\pi}\Rightarrow Ka=\frac{2.2}{\pi} \qquad (11)$$

for the hybrid SLL we have

$$Kd=KaKf$$
$$=Ka(1)(1/2)(1/2)(1/2)=\frac{1}{2\pi}\Rightarrow Ka=\frac{2.2}{\pi} \qquad (12)$$

for the combinational SLL we have

$$Kd=KaKf=Ka\frac{1}{\pi}=\frac{1}{2\pi}\Rightarrow Ka=0.5 \qquad (13)$$

and for the sequential SLL we have

$$Kd=KaKf=Ka\frac{1}{2\pi}=\frac{1}{2\pi}\Rightarrow Ka=1 \qquad (14)$$

This formulas can be used in other synchronizers.

D. Results

We studied the jitter-noise behavior of four closed loop symbol synchronizers in two configurations.

Fig.10 shows the jitter-noise curves of the four synchronizers without any VCO slope transition reduction (normal configuration).

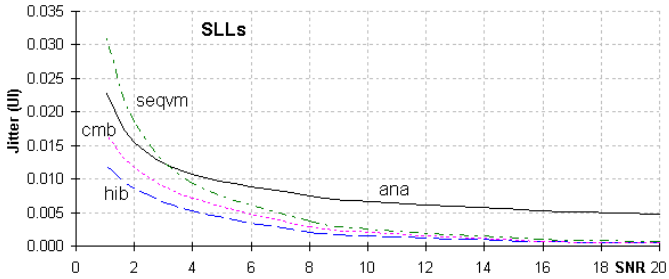

Fig.10 Jitter of the four synchronizers without reduction (a)

We verify that, for high SNR (SNR>4), the synchronizers with limiter in the input (hybrid, combinational and sequential) perform better than the synchronizer without limiter in the input (analog).

For low SNR (SNR<4), the sequential synchronizer (with memory) begins with synchronism problems and therefore performs worst than the others. This disadvantage can be minimized with a prefilter.

Fig.11 shows the jitter-noise curves of the four synchronizers with some VCO slope transition reduction (reduced configuration).

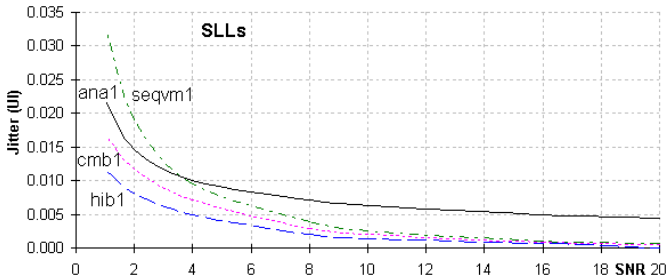

Fig.11 Jitter of the four synchronizers with reduction (b)

For high SNR, the synchronizers with limiter in the input are advantageous over the one without limiter in the input.

For low SNR, the synchronizer without memory is advantageous over the synchronizer with memory. However this disadvantageous of the sequential synchronizer can be minimized with a prefilter.

So, we verify that a little reduction of the clock transition slope doesn't affect significantly the jitter-noise curves.

V. CONCLUSIONS

We tested four synchronizers, namely the analog, hybrid, combinational and sequential in two different configurations. In the first one, the clock is normally fed back and in the second one its transition slope is reduced.

The results show that, in the normal configuration, for high SNR (SNR>4) the synchronizers with limiter in the input (hybrid, combinational and sequential) perform better than the synchronizer without limiter in the input (analog). This is comprehensible because the synchronizers with limiter have noise margin, that ignore low noise quantities, whereas it is token in account by the synchronizer without limiter. For low SNR (SNR<4), the synchronizer with memory (sequential comparator) is disadvantageous relatively to the synchronizers without memory (analog, hybrid and combinational comparators). This is comprehensible because the sequential can enter in the error state increasing the jitter. This disadvantage can be minimized with the prefilter.

In the reduced configuration, with a little reduction of the clock transition slope, the results are not significantly affected.

VI. ACKNOWLEDGMENTS

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