Automatic Potentialities of the Sequential Symbol Synchronizer

António D. Reis*, José F. Rocha, Atilio S. Gameiro, José P. Carvalho*

*Dep. de Fisica, Universidade da Beira Interior Covilhã, 6200 Covilhã, Portugal

Resumo **- Neste artigo apresentamos quatro tipos de sincronizadores de símbolo normais, nomeadamente o analógico, o híbrido, o combinacional e o sequencial.**

O sincronizador sequencial normal tem potencialidades que permitem obter o correspondente sincronizador de símbolo automático. Também o sincronizador sequencial normal tem potencialidades que permitem obter versãoes a operar a submultiplos da taxa de transmissão.

O principal objectivo deste é estudar os vários sincronizadores de símbolo, obter as correspondentes versões automáticas e outras versões operando a submultiplos da taxa de transmissão e estabelecer comparações de performance.

Palavras chave: **Sincronismo em Comunicações Digitais**

Abstract **- In this paper we present four types of normal symbol synchronizers, namely the analog, the hybrid, the combinational and the sequential.**

The normal sequential synchronizer has potentialities that permits to obtain the correspondent automatic symbol synchronizer. Also the normal sequential synchronizer has potentialities that permits to obtain versions operating at submultiples of the transmission rate.

The main objective is to study the various symbol synchronizers, obtain the corespondent automatic versions and others versions operating at submultiples of the transmission rate and to establish performance comparisons.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

Before, we studied four synchronizer types, namely the analog, the hybrid, the combinational and the sequential.

The sequential is a synchronizer, whose signal comparator has memory. This characteristics provides special capacities permitting to create the automatic version and operations at sub data rates.

Fig.1 shows the normal sequential version where a variable pulse Pv produced by a flip flop with exor is compared against a fixed pulse Pf produced by a delay with exor.

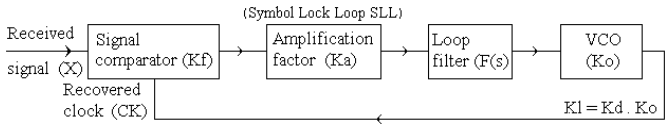

Fig.1 General symbol synchronizer

In perfect synchronism the variable pulse and the fixed one begin and finishes at the same time.

Out of synchronism, the two pulses begin at the same time but finishes at different time, depending on the delay or advance of the clock relatively to the data.

Firstly, we present the four types of synchronizers (analog, hybrid, combinational and sequential).

After, we present a correspondent version totally automatic..

And then we present a normal correspondent version operating internally at sub data rates of the external bit rate. So this synchronizer has the potential of operate internally at low clock speed but transmitting externally at high transmission rate.

Then, we show the design, tests and results with some comparisons [1, 6, 7, 8].

Finally, we present the main conclusions.

II. SYMBOL SYNCHRONIZER TYPES

The four topologies of closed loop symbol synchronizers are got introducing the respective signal comparator [8].

A. Analog synchronizer

Fig.2 shows the analog closed loop synchronizer that is composed by the analog signal comparator, amplification factor, filter and VCO.

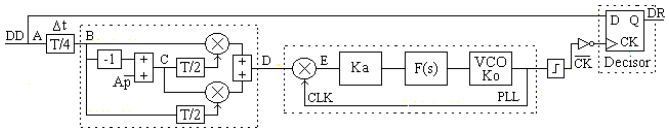

Fig.2 Normal analog symbol synchronizer

The input signal of the SLL and the VCO output, at the signal comparator input, are both analog.

B. Hybrid synchronizer

Fig.3 shows the hybrid closed loop synchronizer that is composed by the hybrid signal comparator, amplification factor, filter and VCO.

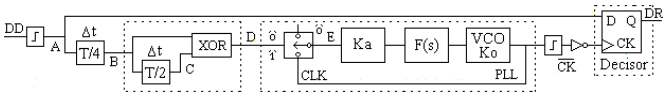

Fig.3 Normal hybrid symbol synchronizer

The input signal of the SLL is digital but the VCO output is still analog.

C. Combinational synchronizer

Fig.4 shows the combinational closed loop synchronizer that is composed by the combinational signal comparator, amplification factor, filter and VCO.

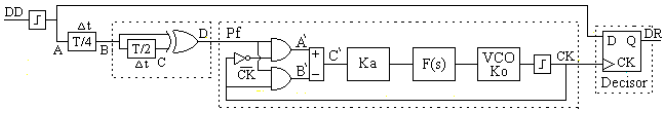

Fig.4 Normal combinational symbol synchronizer

The two inputs of the signal comparator are both digital and its output is only function of the entries.

D. Sequential synchronizer

Fig.5 shows the sequential closed loop synchronizer that is composed by the sequential signal comparator, amplification factor, filter and VCO [2].

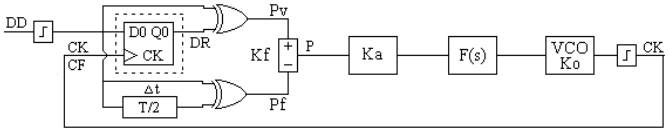

Fig.5 Normal sequential symbol synchronizer

The two inputs of the signal comparator are both digital but now its output depends simultaneously on the two entries and also on the phase comparator state (memory).

III. AUTOMATIC VERSION

The sequential synchronizer is based on the comparison of a variable pulse with a fixed one. In the normal version the fixed pulse was produced by a delay with flip flop. It is possible to substitute the delay by another flip flop and then no more previously manual adjust is needed.

Fig.6 shows the automatic version where the fixed pulse is automatically produced [4].

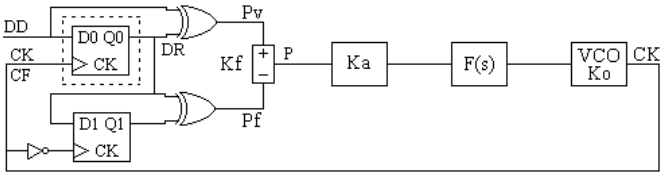

Fig.6 Automatic version of the sequential synchronizer

The variable pulse begins on the data transition and finishes on the next clock positive transition. The fixed pulse [T/2] begins in the clock positive transition and finishes on the next clock negative transition. In correct synchronism the variable pulse is sensibly equal to the fixed one but with different phases.

IV. SUB DATA RATE VERSION

The sequential synchronizer has capacities that permits to operate internally at low speed and transmit externally at high bit rate. This is performed by the parallel processing with each flip flop operating alternatively.

Fig.7 shows the clock synchronizer operating internally at half of the external bit rate [3].

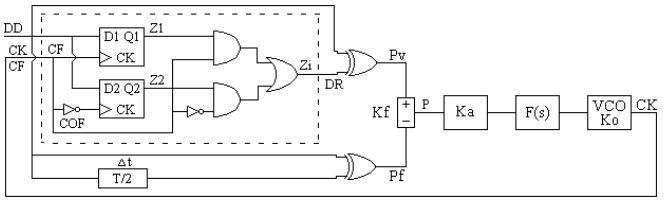

Fig.7 Half frequency operation version of the bit rate

The two flip flop operating only at half of the bit rate is equal to a single flip flop operating at the proper bit rate. The global effect on the bit rate is the sum of the two flip flop clock speed.

It is easy to create versions operating at a submultiple frequency $1/2^n$ of the data rate.

V. DESIGN, TESTS AND RESULTS

A. Test setup

Fig.8 shows the setup that we used to get the jitter-noise curves of the various synchronizers [5].

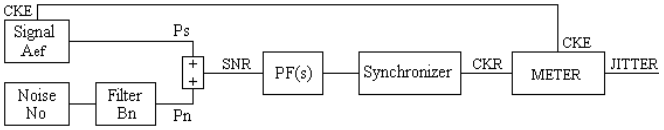

Fig.8 Block diagram of the test setup

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS

amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

The prefilter is not used here, but can be useful in system with high noise quantities (PF(s)=1).

B. Jitter measurer

Fig.9 shows the jitter measurer (METTER) that consists of a RS flip-flop which detects the variable phase of the recovered clock (VCO) relatively to the fixed phase of the emitter clock.

This relative phase variation is the recovered clock jitter.

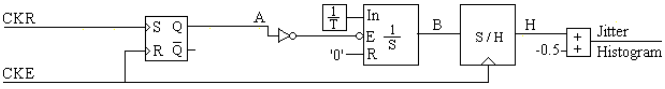

Fig.9 The jitter measurer

The others blocks convert this phase variation into an amplitude variation, which is the jitter histogram.

Fig.10 shows the waveforms that illustrate the operation mode of the jitter measurer.

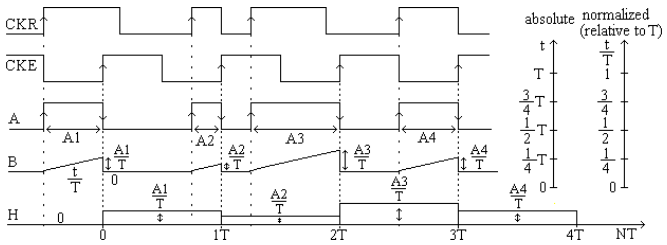

Fig.10 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving the average m, jitter variance in squared radians σ_n^2, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

We have used also others jitter measurers with similar results.

C. Loop parameters design

To establish guaranteed comparisons it is necessary to test all the synchronizers in equal conditions.

We use a normalized transmission rate tx=1baud (fo=1Hz) what facilitates the analyses and allows one more easy extrapolation for other rhythms of transmission. We use an equivalent external noise bandwidth Bn=5Hz for all SLL. For the closed loop symbol synchronizers SLL, we use a loop noise bandwidth Bl=0.02Hz.

For analog SLL, the relation between signal to noise ratio SNR and jitter variance σn is $SNR=Aef^2/No.Bn=A_{ef}^2/(2\sigma n^2.\Delta\tau.Bn)=(0.5)^2/(2\sigma n^2*10^{-3}*5)=25/\sigma n^2$. This relation is more complicated for the others symbol synchronizers.

We will now present the loop parameters design for the various PLLs considering the first (1st) and the second order loop (2nd).

- 1st order loop:

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st order is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \qquad (1)$$

the loop noise bandwidth for the SLLs is

$$B1=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \qquad (2)$$

so for the analog SLL with Km=1, A=1/2, B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (3)$$

for the hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (4)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/\pi)2\pi}{4}=0.02Hz \Rightarrow Ka=0.04 \qquad (5)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/2\pi)2\pi}{4}=0.02 \Rightarrow 0.08 \qquad (6)$$

This formulas are useful in synchronizers design

- 2nd order loop:

The transfer function with $F(s)=\frac{1+sT2}{sT1}$ is

$$H(s)=\frac{sKdKo(T2/T1)+KdKo/T1}{s+sKdKo(T2/T1)+KdKo/T1} \qquad (7)$$

$$=\frac{sA+B}{s^2+s2\xi Wn+Wn^2} \qquad (8)$$

and the loop noise bandwidth is

$$B1=\frac{\xi Wn}{2}\left(1+\frac{1}{4\xi^2}\right) \qquad (9)$$

Taking (ξ=1 and Bl=0.02) and solving the above equations we obtain for F(s)

$$F(s)=\frac{1+s63}{s977} \qquad (10)$$

so for the analog SLL we have

$$Kd = kaKf = Ka(1)(1/2)(1/2) = \frac{1}{2\pi} \Rightarrow Ka = \frac{2.2}{\pi} \qquad (11)$$

for the hybrid SLL we have

$$Kd = kaKf = Ka(1)(1/2)(0.45) = \frac{1}{2\pi} \Rightarrow Ka = \frac{2.2}{\pi} \qquad (12)$$

for the combinational SLL we have

$$Kd = kaKf = \frac{Ka}{\pi} = \frac{1}{2\pi} \Rightarrow Ka = 0.5 \qquad (14)$$

and for the sequential SLL we have

$$Kd = kaKf = \frac{Ka}{\pi} = \frac{1}{2\pi} \Rightarrow Ka = 1 \qquad (14)$$

This formulas can be used in others synchronizers.

D. Results

We studied the potentialities of the normal sequential synchronizer in order to provide an automatic version and other operating internally at half of the transmission rate.

Fig.11 shows the jitter-noise curves of the normal/manual (man) and automatic (aut) sequential synchronizers.

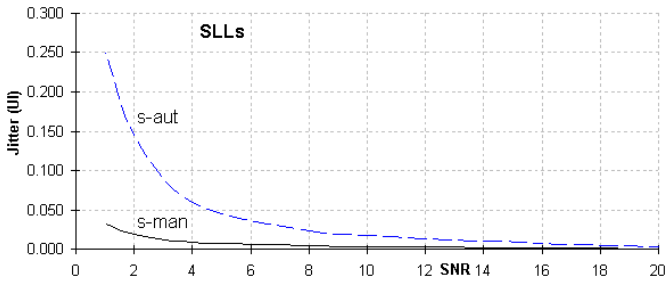

Fig.11 Analog synchronizer with the four prefilters PF(s)

We verify that for high SNR (SNR>4) the two curves are identical.

However for low SNR (SNR<4) the normal version has some advantage over the automatic one.

Fig.12 shows the jitter-noise curves of the normal/manual (man) and normal half rate (tx/2) sequential synchronizers.

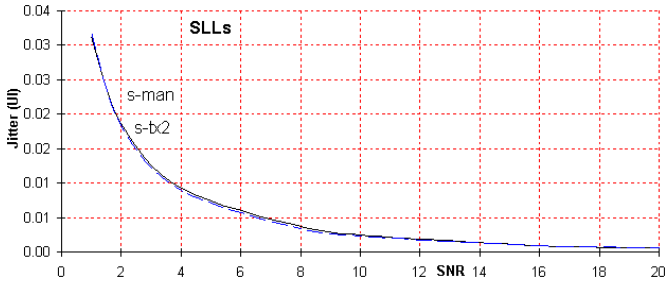

Fig.12 Hybrid synchronizer with the four prefilters

We verify that the two curves are identical for low and high SNR.

VI. CONCLUSIONS

We studied the normal sequential symbol synchronizer, we saw its potentialities and capacities to get the automatic version and an half rate operation version.

We verify that, for high SNR (SNR>4), the automatic version has a similar performance with the normal one. However for low SNR (SNR<4), the automatic version is disadvantageous relatively the normal one. This is due to propagation error state of the signal comparator. So for low SNR the normal version must be used due to its better performance, but for high SNR the automatic version must be used due to its better adjust.

Also we verify that the normal and the half rate version are identical performance for low and high SNR. It is comprehensible because the state number and gain of both signal comparators is equal.

Globally, we noted that for good transmission links (SNR>8) the various versions are similar.

VII. ACKNOWLEDGMENTS

The authors are thankful to the program FCT (Foundation for sCience and Technology).

VIII. REFERENCES

[1] Werner Rosenkranz, “Phase Locked Loops with limiter phase detectors in the presence of noise”, IEEE Transactions on Communications com-30. October 1982.

[2] Charles R. Hogge, “A Self Correcting Clock Recovery Circuit”, Journal of Lightwave Technology, Dec. 1985.

[3] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho “Bit Synchronizer Operating at Half Rate”, II Conference on Telecommunications p.550, Sesimbra-PT 15-16 April 1999.

[4] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, “Manual and Automatic Data Synchronizers”, 7th International Conference on Telecommunications p.1076, Acapulco-MX 22-25 May 2000.

[5] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho “A New Technique to Measure the Jitter”, III Conference on Telecommunications p.64, F. Foz-PT 23-24 April 2001.

[6] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, “Open Loop Symbol Synchronizers”, 9th International Conference on Telecommunications p.286, Beijing-CN 23-26 June 2002.

[7] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, “Mixed Loop Symbol Synchronizers”, 3th International Symp. on Communication Systems Networks and Digital Signal Processing p.324, Stafford-UK 15-17 July 2002.

[8] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho “Closed Loop Symbol Synchronizers with Prefilter”, IV Conference on Telecommunications p.433, Aveiro-PT 18-20 June 2003.