Asynchronous Capacities of the Sequential Symbol Synchronizer

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Resumo **- Neste artigo apresentamos quatro tipos de sincronizadores de símbolo normais, nomeadamente o analógico, o híbrido, o combinacional e o sequencial.**

O sincronizador sequencial síncrono tem capacidades que permitem obter a correspondente versão assíncrona. Assim o flip flop é substituido por lógica com realimentação. Então todos os sincronizadores usam somente portas lógicas.

O principal objectivo é desenvolver o sincronizador sequencial assíncrono e depois estudar e comparar a performance das duas vesrsões.

Palavras chave: **Sincronismo em Comunicações Digitais**

Abstract **- In this paper we present four types of normal symbol synchronizers, namely the analog, the hybrid, the combinational and the sequential.**

The synchronous sequential synchronizer has capacities that permits to obtain the correspondent asynchronous version. So the flip flop is substituted by logic with feedback. Then all the synchronizers use only logic gates.

The main objective is to develop the synchronous sequential synchronizer and then to study and compare the performance of the two versions.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

Before, we studied four synchronizer types, namely the analog, the hybrid, the combinational and the sequential.

The synchronizers analog, hybrid, and combinational are implemented with logic gates but the sequential one is implemented with logic gates and flip flops.

As, at low frequencies, the synchronous sequential synchronizer seems disadvantageous relatively to the others, then we go develop the correspondent asynchronous version that are implemented only with logic gates with feedback. So all the synchronizers are implemented only with logic gates.

Fig.1 shows the general block diagram of the closed loop synchronizers.

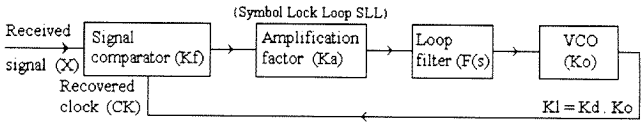

Fig.1 General closed loop synchronizer

The closed loop synchronizer is composed by the signal comparator, amplification factor, filter and VCO.

The great difference between the various synchronizers is inside the signal comparator. The others blocks are identical.

Firstly, we present the four types of synchronizers (analog, hybrid, combinational and sequential).

Next, we go present the correspondent asynchronous sequential version.

After, we show the design, tests and results with some comparisons [1, 6, 7, 8].

Finally, we present the main conclusions.

II. CLOSED SYMBOL SYNCHRONIZER TYPES

The four types of closed loop symbol synchronizers are got inserting the appropriate signal comparator [3, 4].

A. Analog synchronizer

Fig.2 shows the analog synchronizer, in which, the signal comparator is composed by three multipliers, two T/2 delays and inverter.

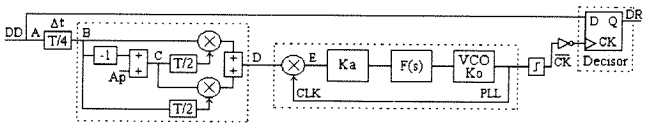

Fig.2 Analog symbol synchronizer

The main input signal and the VCO output, at the signal comparator inputs, are both analog.

B. Hybrid synchronizer

Fig.3 shows the hybrid synchronizer, in which, the signal comparator is composed by a triple switch, an exor and two delays.

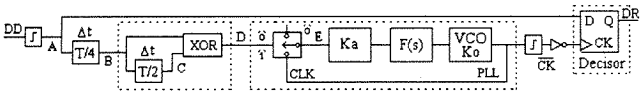

Fig.3 Hybrid symbol synchronizer

The main input signal is already digital but the VCO output is still analog.

C. Combinational synchronizer

Fig.4 shows the combinational synchronizer, in which, the signal comparator is composed by a Mux (two ANDs) with adder, an exor and two delays (T/4, T/2).

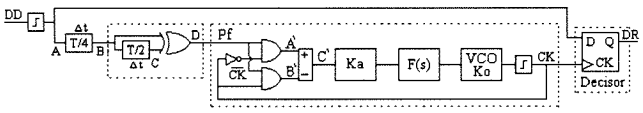

Fig.4 Combinational symbol synchronizer

The two inputs (main input and VCO output) of the signal comparator are both digital. The output is only function of the entries.

D. Sequential synchronizer

Fig.5 shows the sequential synchronizer, in which, the signal comparator is composed by one flip flop with exor and a delay with exor, followed of an adder [2].

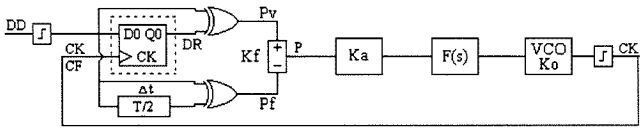

Fig.5 Synchronous sequential symbol synchronizer

The two inputs (main input and VCO output) of the signal comparator are both digital. However now, the output is simultaneously function of the two entries and also of the signal comparator state (memory).

III. ASYNCHRONOUS SEQUENTIAL VERSION

The difference between the synchronous and asynchronous versions can be evidenced by the CS dush outlined rectangle of Fig.6. The CF circuit determines the version of the symbol synchronizer that can be synchronous or asynchronous.

Fig.6 shows the synchronous version when the CF dush outlined is a flip flop as shown in Fig.5 [4].

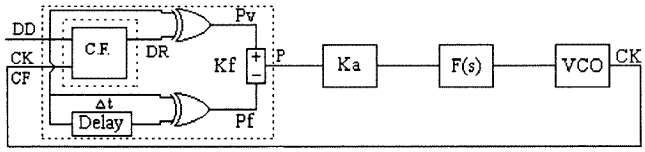

Fig.6 Synchronous version of the sequential synchronizer

The synchronous version is easier to implement, anyway we must obtain the asynchronous version, to make the performance comparisons.

Fig.7 shows the CF circuit implemented with feedback logic. So if this circuit corresponds to the CF circuit of Fig.6 we have the asynchronous sequential synchronizer [4].

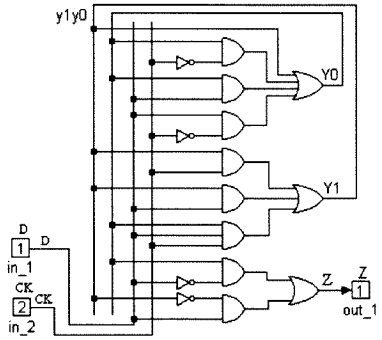

Fig.7 Asynchronous version of the sequential synchronizer

This two versions will be implemented and tested to see its jitter-noise performance.

IV. DESIGN, TESTS AND RESULTS

A. Test setup

Fig.8 shows the setup that we used to get the jitter-noise curves of the various synchronizers [5].

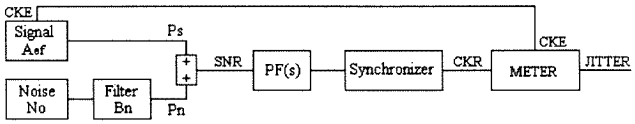

Fig.8 Block diagram of the test setup

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

The prefilter is not used here, but can be useful in system with high noise quantities (PF(s)=1).

B. Jitter measurer

Fig.9 shows the jitter measurer (METTER) that consists of a RS flip-flop which detects the variable phase of the recovered clock (VCO) relatively to the fixed phase of the emitter clock.

This relative phase variation is the recovered clock jitter.

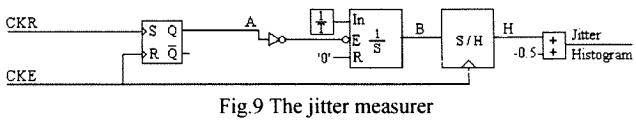

Fig.9 The jitter measurer

The others blocks convert this phase variation into an amplitude variation, which is the jitter histogram.

Fig.10 shows the waveforms that illustrate the operation mode of the jitter measurer.

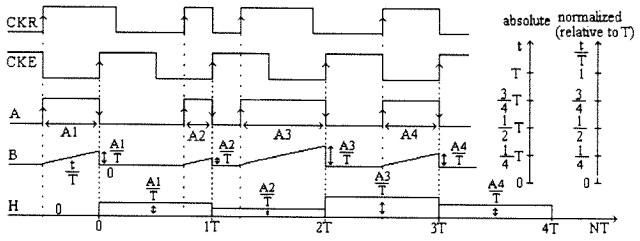

Fig.10 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving the average m, jitter variance in squared radians σ_n^2, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

We have used also others jitter measurers with similar results.

C. Loop parameters design

To establish guaranteed comparisons it is necessary to test all the synchronizers in equal conditions.

We use a normalized transmission rate tx=1baud (fo=1Hz) what facilitates the analyses and allows one more easy extrapolation for other rhythms of transmission. We use an equivalent external noise bandwidth Bn=5Hz for all SLL. For the closed loop symbol synchronizers SLL, we use a loop noise bandwidth Bl=0.02Hz.

For analog SLL, the relation between signal to noise ratio SNR and jitter variance σn is $SNR=Aef^2/No.Bn=A_{ef}^2/(2\sigma n^2.\Delta\tau.Bn)=(0.5)^2/(2\sigma n^2*10^{-3}*5)=25/\sigma n^2$. This relation is more complicated for the others symbol synchronizers.

We will now present the loop parameters design for the various PLLs considering the first (1st) and the second order loop (2nd).

- 1st order loop:

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st order is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \qquad (1)$$

the loop noise bandwidth for the SLLs is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02\text{Hz} \qquad (2)$$

so for the analog SLL with Km=1, A=1/2, B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (3)$$

for the hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz \Rightarrow Ka=0.08\frac{2.2}{\pi} \qquad (4)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/\pi)2\pi}{4}=0.02Hz \Rightarrow Ka=0.04 \qquad (5)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/2\pi)2\pi}{4}=0.02Hz \Rightarrow Ka=0.08 \qquad (6)$$

This formulas are useful in synchronizers design

- 2nd order loop:

The transfer function with F(s) = $F(s)=\frac{1+sT2}{sT1}$ is

$$H(s)=\frac{sKdKo(T2/T1)+KdKo/T1}{s+sKdKo(T2/T1)+KdKo/T1} \qquad (7)$$

$$=\frac{sA+B}{s^2+s2\xi Wn+Wn^2} \qquad (8)$$

and the loop noise bandwidth is

$$Bl=\frac{\xi Wn}{2}\left(1+\frac{1}{4\xi^2}\right) \qquad (9)$$

Taking (ξ=1 and Bl=0.02) and solving the above equations we obtain for F(s)

$$F(s)=\frac{1+s63}{s977} \qquad (10)$$

so for the analog SLL we have

$$Kd = KaKf = Ka(1)(1/2)(1/2)=\frac{1}{2\pi}\Rightarrow Ka=\frac{2.2}{\pi} \qquad (11)$$

for the hybrid SLL we have

$$Kd = KaKf = Ka(1)(1/2)(1/0.45)=\frac{1}{2\pi}\Rightarrow Ka=\frac{2.2}{\pi} \qquad (12)$$

for the combinational SLL we have

$$Kd = KaKf = \frac{Ka}{\pi}=\frac{1}{2\pi}\Rightarrow Ka=0.5 \qquad (13)$$

and for the sequential SLL we have

$$Kd = KaKf = \frac{Ka}{2\pi}=\frac{1}{2\pi}\Rightarrow Ka=1 \qquad (14)$$

This formulas can be used in others synchronizers.

D. Results

We studied four synchronizers types, namely the analog (an), the hybrid (hib), the combinational (cmb) and the sequential (seq). Then we taked this synchronous sequential synchronizer (sinc) and we create the correspondent asynchronous sequential synchronizer (asinc)

Fig.11 shows the jitter-noise curves of the four synchronizer types (ana, hib, cmb, seq).

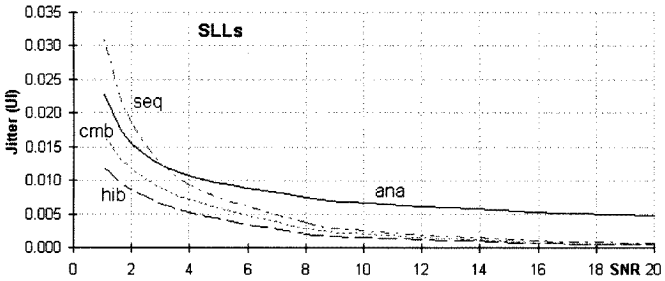

Fig.11 Jitter curves of synchronizers (ana, hib, cmb, seq)

We verify that generically the jitter UI diminishes when the signal to noise ratio SNR increases.

For low SNR (SNR<4), the synchronizer without input limiter (analog) is advantageous over the others with input limiter (hybrid, combinational, sequential)

However for high SNR (SNR>4) the synchronizer without input limiter is disadvantageous over the others with input limiter.

Fig.12 shows the jitter-noise curves of the two synchronizer versions (sinc, asinc).

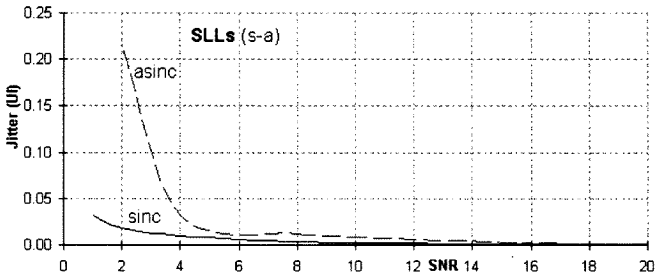

Fig.12 Jitter-noise curves of synchronizers (sinc, asinc)

We verify that, for low SNR (SNR<5) the synchronous synchronizer is advantageous over the asynchronous one.

However, for high SNR (SNR>5), the synchronous and asynchronous synchronizers have identical jitter-noise performance.

V. CONCLUSIONS

We studied four symbol synchronizers, namely the analog (ana), the hybrid (hib), the combinational (cmb) and the sequential (seq).

Then we taked the capacities of the synchronous sequential synchronizer (sinc) and we developed the asynchronous version (asinc).

In the synchronizers (ana, hib, cmb, seq) we verify that for low SNR the synchronizers without input limiter (ana) is advantageous over the others with input limiter (hib, cmb, seq). This is due to the noise spikes that provokes random gate commutations. The worst case is the sequential synchronizer but it can be minimized with a prefilter. However, for high SNR (SNR>4), the synchronizer without input limiter is disadvantageous over the others due to the noise margin of the limiter gates.

In the synchronizers (sinc, asinc), we verify that for low SNR (SNR<5), the synchronous synchronizer is advantageous over the asynchronous one due to its inter states critical runs, that conducts to the error state. However, for high SNR (SNR>5), in which the synchronizers normally operates, the two synchronizers have identical jitter-noise performance. The jitter is only due to the input noise.

Globally, we noted that the jitter UI decreases when the signal to noise rate SNR increases.

ACKNOWLEDGMENTS

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REFERENCES

[1] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Transactions on Communications com-30. October 1982.

[2] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", Journal of Lightwave Technology, Dec. 1985.

[3] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, "Manual and Automatic Data Synchronizers", 7th International Conference on Telecommunications p.1076, Acapulco-MX 22-25 May 2000.

[4] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, "High Data Rate Synchronizers Operating at Low Speed", The 8th IEEE International Conference on Electronics, Circuits and Systems p.1127, Malta-MT 2-5 September 2001.

[5] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "A New Technique to Measure the Jitter", III Conference on Telecommunications p.64, F. Foz-PT 23-24 April 2001.

[6] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, "Open Loop Symbol Synchronizers", 9th International Conference on Telecommunications p.286, Beijing-CN 23-26 June 2002.

[7] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho, "Mixed Loop Symbol Synchronizers", 3th International Symp. on Communication Systems Networks and Digital Signal Processing p.324, Stafford-UK 15-17 July 2002.

[8] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "Closed Loop Symbol Synchronizers with Prefilter", IV Conference on Telecommunications p.433, Aveiro-PT 18-20 June 2003.