Wave and Symbol Synchronizers

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Resumo **- Neste artigo apresentamos quatro sincronizadores de onda e quatro sincronizadores de símbolo: analógico, híbrido, combinacional e sequencial. Todos eles são da classe malha fechada.**

Os sincronizadores de onda estão vocacionados para se sincronizarem com ondas ou sinais de fase deterministica.

Os sincronizadores de símbolo estão vocacionados para se sincronizarem com símbolos ou sinais de fase aleatória.

O principal objectivo é estudar e comparar a performance dos diferentes sincronizadores de onda e de símbolo.

Palavras chave: Sincronismo em Comunicações Digitais

Abstract **- In this paper we present four wave synchronizers and four symbol synchronizers: analog, hybrid, combinational and sequential. All them are of the class closed loop.**

The wave synchronizers are vacated to synchronize with waves or signals with deterministic phase/ transition.

The symbol synchronizers are vacated to synchronize with symbols or signals with random phase/ transition.

The main objective is to study and compare the performance of the different wave and symbol synchronizers.

Key words: Synchronism in Digital Communications

I. INTRODUCTION

Here, we present four wave phase lock loop WPLL or only PLL and four symbol phase lock loop SPLL or only SLL.

Fig.1 shows the general block diagram of the closed loop wave and symbol synchronizers [6, 7, 8].

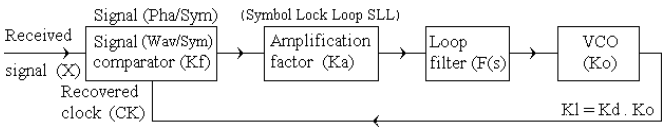

Fig.1 General closed loop synchronizer

The closed loop wave and symbol synchronizer is composed by the signal (wave/ symbol) comparator, amplification factor, filter and VCO.

The wave/ symbol comparator compares the VCO phase with the one of the input signal.

The amplification factor controls the loop characteristics.

The loop filter capts the DC voltage and eliminates the high frequencies.

The VCO is an oscillator controlled by voltage.

The great difference between the various synchronizers is inside the signal comparator. The others blocks are identical.

Firstly, we present the four wave phase lock loop and four symbol phase lock loop synchronizers (ana, hib, cmb, seq) then, we show the design, tests and results with some comparisons [1, 2, 6, 7, 8].

Finally, we present the main conclusions.

II. WAVE SYNCHRONIZER TYPES

First we present the four wave synchronizers: the analog, the hybrid, the combinational and the sequential [3].

A. Analog WPLL/ PLL

Fig.2 shows the analog PLL. The phase comparator is based on a linear multiplier (ideal multiplier).

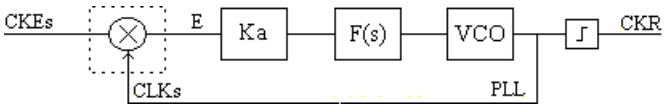

Fig.2 Analog phase synchronizer

The input signal and the VCO output at the phase comparator are both analog.

B. Hybrid WPLL/ PLL

Fig.3 shows the hybrid PLL. The phase comparator is based on a nonlinear multiplier (switch). In practice, due to its simple implementation, this common multiplier is frequently used.

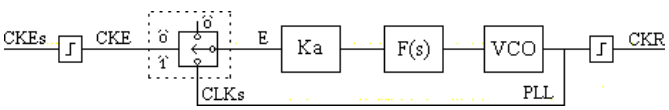

Fig.3 Hybrid phase synchronizer

The input signal is digital but the VCO output is still analog.

C. Combinational WPLL/ PLL

Fig.4 shows the combinational PLL. The phase comparator is based on a XNOR gate. The XNOR is equivalent to an ideal multiplier with limiters in the two inputs.

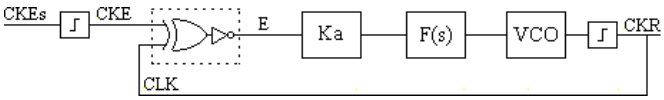

Fig.4 Combinational phase synchronizer

The two phase comparator inputs are both digital and its output is only function of the two inputs.

D. Sequential WPLL/ PLL

Fig.5 shows the sequential PLL. The phase comparator is based on a RS Flip-Flop (edge-triggered) indicated by triangles in the two inputs. A RS Latch would be presented without triangles.

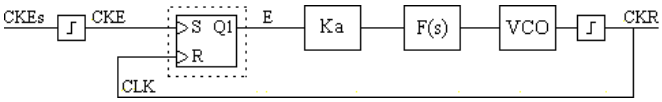

Fig.5 Sequential phase synchronizer

The two inputs of the phase comparator are both digital but now its output depends simultaneously on the two entries and the phase comparator state (memory).

IV. SYMBOL SYNCHRONIZER TYPES

In this section we recall the four symbol synchronizers [4]: the analog, the hybrid, the combinational and the sequential

A. Analog SPLL/ SLL

Fig.6 shows the analog type, in which the symbol comparator is composed by three analog multipliers (ideal multiplier) two for data transitions and one for comparison.

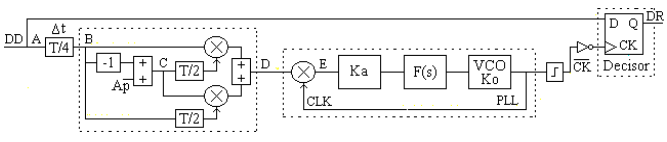

Fig.6 Analog symbol synchronizer

The main input and VCO output are both analog at the symbol comparator..

B. Hybrid SPLL/ SLL

Fig.7 shows the hybrid type, in which the symbol comparator is composed by a XOR with delay followed of an analog multiplier or switch (real multiplier).

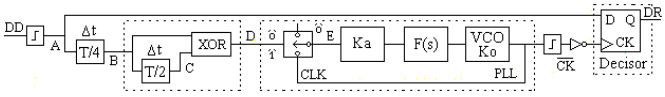

Fig.7 Hybrid symbol synchronizer

The main input signal is already digital but the VCO output is still analog at the symbol comparator.

C. Combinational SPLL/ SLL

Fig.8 shows the combinational type, in which the symbol comparator is composed by a XOR with delay followed of a digital demux.

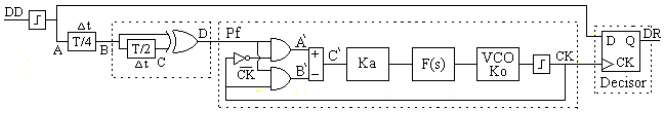

Fig.8 Combinational symbol synchronizer

The symbol comparator inputs are both digital and its output is only function of the two present inputs.

D. Sequential SPLL/ SLL

Fig.9 shows the sequential type, in which the symbol comparator is composed by a XOR with a flip flop (variable pulse Pv) and a XOR with a delay (fixed pulse Pf) [2].

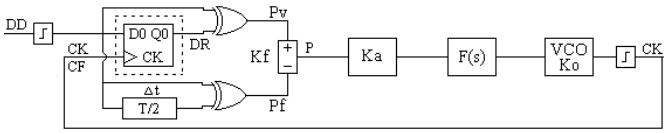

Fig.9 Sequential symbol synchronizer

The symbol comparator inputs are both digital but now its output is simultaneously function of the two present inputs and also symbol comparator state (memory).

IV. DESIGN, TESTS AND RESULTS

A. Test setup

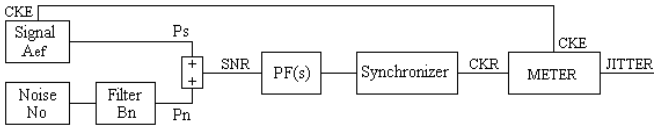

Fig.10 Block diagram of the test setup

Fig.10 shows the setup that we used to get the jitter-noise curves of the various synchronizers [5].

The signal to noise ratio SNR is given by Ps/Pn, where Ps is the signal power and Pn is the noise power. They are defined as $Ps=A_{ef}^2$ and $Pn=No.Bn=2\sigma_n^2\Delta\tau$ Bn. A_{ef} is the RMS amplitude, Bn is the external noise bandwidth, No is the noise power spectral density, σ_n is the noise standard deviation and $\Delta\tau$ is the sampling period (inverse of samples per unit time).

The prefilter is not used here, but can be useful in systems with high noise quantities (PF(s)=1).

B. Jitter measurer

Fig.11 shows the jitter measurer (METTER) that consists of a RS flip-flop which detects the variable phase of the recovered clock (VCO) relatively to the fixed phase of the emitter clock.

This relative phase variation is the recovered clock jitter.

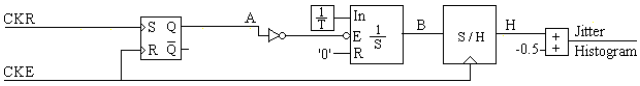

Fig.11 The jitter measurer

The others blocks convert this phase variation into an amplitude variation, which is the jitter histogram. Fig.12 shows the waveforms that illustrate the operation mode of the jitter measurer.

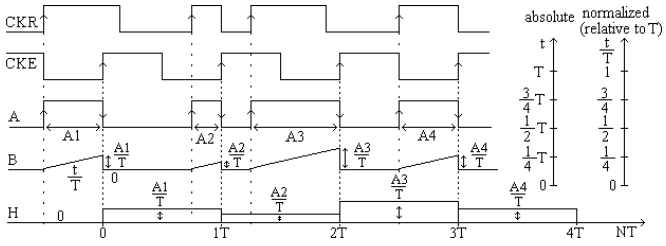

Fig.12 Waveforms at the jitter measurer

The jitter histogram is then sampled and processed by an appropriated program giving the average m, jitter variance in squared radians σ_n^2, jitter standard deviation in unit intervals root mean squared UIRMS and jitter standard deviation in unit intervals peak to peak UIPP.

We have used also others jitter measurers with similar results.

C. Loop parameters design

To establish guaranteed comparisons it is necessary to test all the synchronizers in equal conditions.

We use a normalized transmission rate tx=1baud (fo=1Hz) what facilitates the analyses and allows one more easy extrapolation for other rhythms of transmission. We use an equivalent external noise bandwidth Bn=5Hz for all SLL. For the closed loop symbol synchronizers SLL, we use a loop noise bandwidth Bl=0.02Hz.

For analog SLL, the relation between signal to noise ratio SNR and jitter variance σn is $SNR=Aef^2/No.Bn=A_{ef}^2/(2\sigma n^2.\Delta\tau.Bn)=(0.5)^2/(2\sigma n^2*10^{-3}*5)=25/\sigma n^2$. This relation is more complicated for the others symbol synchronizers.

We will now present the loop parameters design for the various PLLs considering the first (1st) and the second order loop (2nd).

- 1st order loop:

In the 1st order loop, the filter F(s)=0.5Hz eliminates only the high frequency, but maintain the loop characteristics. This cutoff frequency F(s)=0.5Hz is 25 times higher than Bl=0.02Hz. Then the transfer function of the 1st order is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth for the SLLs is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

so for the analog SLL with Km=1, A=1/2, B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz;\quad Ka=0.0\frac{2.2}{\pi} \quad (3)$$

for the hybrid SLL, with Km=1, A=1/2 and B=0.45 we have

$$Ka\frac{KmABKo}{4}=0.02Hz;\quad Ka=0.08\frac{2.2}{\pi} \quad (4)$$

for the combinational SLL (Kf=1/π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/\pi)2\pi}{4}=0.02Hz;\quad Ka=0.04 \quad (5)$$

and for the sequential SLL (Kf=1/2π) we have

$$Ka\frac{KfKo}{4}=Ka\frac{(1/2\pi)2\pi}{4}=0.02Hz;\quad Ka=0.08 \quad (6)$$

This formulas are useful in synchronizers design

- 2nd order loop:

The transfer function with $F(s)=\frac{1+sT2}{sT1}$ is

$$H(s)=\frac{sKdKo(T2/T1)+KdKo/T1}{s+sKdKo(T2/T1)+KdKo/T1} \quad (7)$$

$$=\frac{sA+B}{s^2+s2\xi Wn+Wn^2} \quad (8)$$

and the loop noise bandwidth is

$$Bl=\frac{\xi Wn}{2}\left(1+\frac{1}{4\xi^2}\right) \quad (9)$$

Taking (ξ=1 and Bl=0.02) and solving the above equations we obtain for F(s)

$$F(s)=\frac{1+s63}{s977} \quad (10)$$

so for the analog SLL we have

$$Kd=KaKf=Ka(1)(1/2)(1/2)=\frac{1}{2\pi};\qquad Ka=\frac{2.2}{\pi} \quad (11)$$

for the hybrid SLL we have

$$Kd=KaKf=Ka(1)(1/2)(0.45)=\frac{1}{2\pi};\qquad Ka=\frac{2.2}{\pi} \quad (12)$$

for the combinational SLL we have

$$Kd=KaKf=Ka\frac{1}{\pi}=\frac{1}{2\pi};\quad Ka=0.5 \quad (13)$$

and for the sequential SLL we have

$$Kd=KaKf=Ka\frac{1}{2\pi}=\frac{1}{2\pi};\quad Ka=1 \quad (14)$$

This formulas can be used in others synchronizers.

D. Results

We studied the jitter-noise behavior of four wave and four symbol synchronizers namely the analog (ana), hybrid (hib), combinational (cmb) and the sequential (seq).

Fig.13 shows the jitter-noise curves of the four wave synchronizers (ana, hib, cmb, seq).

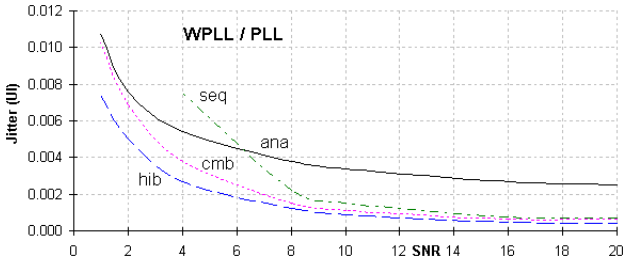

Fig.13 Curves of the wave synchronizers (ana, hib, cmb, seq)

We verify that generically the jitter UI (UIRMS) diminishes when the signal to noise ratio SNR increases.

For low SNR, the synchronizer without input limiter (analog) tends to be advantageous over the others with input limiter (hybrid, combinational, sequential).

However, for high SNR, the synchronizer without input limiter (analog) is disadvantageous over the others with input limiter (hybrid, combinational, sequential).

Fig.14 shows the jitter-noise curves of the four symbol synchronizers (ana, hib, cmb, seq).

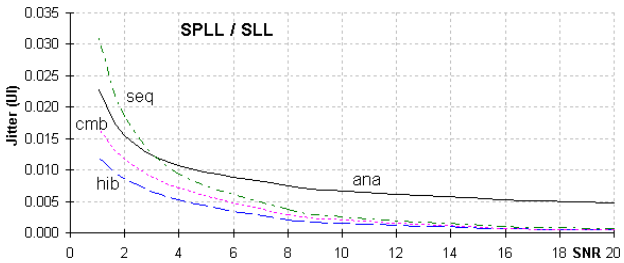

Fig.14 Curves of the symbol synchronizers (ana, hib, cmb, seq)

We verify that generically the jitter UI diminishes when the signal to noise ratio SNR increases.

For low SNR, the synchronizer without input limiter (analog) tends to be advantageous over the others with input limiter (hybrid, combinational, sequential).

However for high SNR the synchronizer without input limiter (analog) is disadvantageous over the others with input limiter (hybrid, combinational, sequential).

VI. CONCLUSIONS

We studied four wave and four symbol synchronizers types namely the analog (ana), hybrid (hib), combinational (cmb) and sequential (seq).

In the synchronizers (ana, hib, cmb, seq) we verify that for low SNR, the synchronizer without input limiter (analog) is advantageous over the others with input limiter (hybrid, combinational, sequential). This is comprehensible because the limiter provokes random gate commutations with noise spikes. However for high SNR the synchronizer without input limiter is disadvantageous over the others. This is comprehensible because the limiter noise margin ignores low noise spikes.

The sequential synchronizer is disadvantageous for low SNR due to its memory, but this problem can be minimized with a prefilter.

VII. ACKNOWLEDGMENTS

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