On the Limit of Operational Amplifiers' Supply Voltage

Rui Martins and G. Schrom[1]
[1] Intel Corporation, Hillsboro, OR, USA

Resumo **- O trabalho apresentado neste artigo analisa o impacto da contínua redução das tensões de alimentação e de threshold dos transístores MOSFET nos circuitos analógicos. O estudo incide sobre o amplificador operacional, bloco principal dos sistemas analógicos, e procura estimar qual será o valor mínimo admissível da sua tensão de alimentação. Para ultrapassar o facto de ainda não existirem tecnologias comerciais optimizadas para 0.5 V, utilizando simuladores de processo e de dispositivos, foi desenvolvida uma tecnologia "virtual" que cumpre essa meta. Com base nesta tecnologia é apresentado um amplificador operacional rail-to-rail que, segundo os resultados das simulações, tem um desempenho similar ao que hoje pode ser obtido (para a mesma potência consumida).**

Abstract **- Power-supply and threshold voltages are getting smaller at every technology node. The impact of this reduction in the main building block of analog circuits, the operational amplifier, is studied. In order to develop a technology which is not yet available, extensive Technology CAD (TCAD) simulations are performed. After process optimization based upon digital circuit objectives, the resulting transistor models are used to build a rail-to-rail (both at input and output) operational amplifier that can operate from a supply voltage as low as 0.5 V. The results suggest that the amplifier's performance is similar to what we can obtain today at much higher supply voltages (for the same power consumption).**

I. INTRODUCTION

Today's standard voltages for powering portable equipment span from 1.2 V (one NiMH cell voltage) to 3.6 V (one Lithium-chemistry based battery cell). Whereas almost all portable equipment takes advantage from advances in the continuous voltage/power reduction of integrated circuits, there are applications that demand the ultimate energy efficiency. Among others, bioelectronic devices implanted in the human body (bionics) and equipment to be powered from a single solar-cell (output voltage is about 0.5 V [1]) require operating voltages lower than the current state of the art.

The driving force for voltage/power reduction is the continuous search for higher performance/power efficiency of digital CMOS circuits. But although it is a common place to say the world is getting more and more digital, there are applications where analog is proving to be competitive, namely in the above mentioned bionics [2]. Therefore designing the ultimate low voltage/low-power consumption operational amplifier, the main building block of analog systems, is a critical issue in this area (and surely in many others). This paper addresses the impact of the foreseeable power-supply voltage reduction in the performance of operational amplifiers. It is organized as follows: the evolution of the CMOS technology is discussed in section II; the simulation methodology is explained in section III; the amplifier circuit is presented is section IV; and finally the results are shown in section V, where some conclusions are drawn and future working directions are put forward.

II. TECHNOLOGY TRENDS

There are several reasons for the continuous supply voltage reduction that started in the early 90's. Among others, it was the absolute necessity of diminishing the dissipated power to limit the integrated circuits' temperature and to guarantee the reliability of devices. The latter reason more than being a consequence of the first one, results from the thinner oxide thickness that comes along with technology scaling. Indeed, the oxide thickness is a cause for one of the most challenging issues the next technology nodes has to cope with: a sharp increase in the transistor's leakage current. The thickness is reduced in order to control the Short-Channel Effects (SFE), but as a side effect, it imposes a higher gate leakage current [3]. Other leakage sources of sub 90 nm transistors are the subthreshold current of an OFF transistor between source and drain, the reverse-bias source/drain junction leakages, the Gate Induced Drain Leakage (GIDL) and punchthrough [4]. The sum effect of all these leakage currents, even with the introduction of new high dielectric (the so called high-K) materials, metal electrodes, channel optimization (halo implantation, retrogade wells) and other techniques, is expected to reach an unacceptable level, which will ultimately mean the end of the conventional bulk CMOS technology [5].

According to the 2005 International Technology Roadmap for Semiconductors (ITRS) [6] conventional bulk CMOS technology will phase off in 2013-2014 being replaced by Ultra-Thin-Body Full Depleted (UTB-FD) and Double-Gate (DG) technologies. But the same document predicts that until that date the conventional bulk CMOS will continuously be updated namely in terms

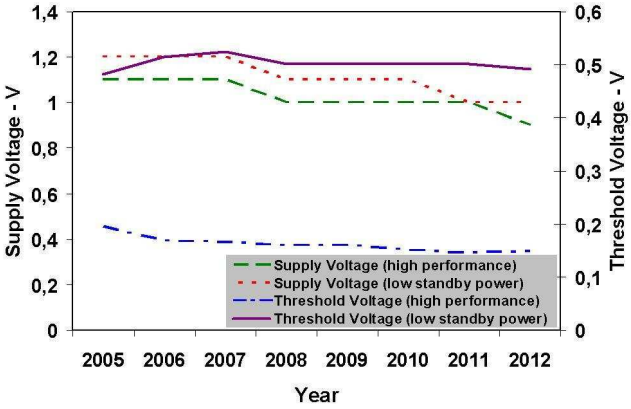

Fig. 1 - Supply-voltage and threshold voltage trend [6].

of power-supply and threshold voltages (Fig. 1). Notice that it shows data for both high performance logic and low standby power applications (as obtained from [6]).

Most of the studied impact of these changes is related to digital high performance circuits (e.g., [7]) and less effort is put into analog circuits. This paper addresses the possible performance of operational amplifiers working at ultra low voltage power supplies implemented in near future technologies. This is achieved by designing an operational amplifier capable of working properly with a power-supply voltage as low as 0.5 V.

Extensive Technology CAD (TCAD) simulations were used to create such a technology: process simulation to build the transistors, device simulation to extract their electrical parameters and finally a circuit simulator to get benchmark results. Notwithstanding the inherent weaknesses of this methodology, it still can prove useful in giving leads to what can be expected to happen in a future not too far!

III. SIMULATION METHODOLOGY

Reference [6] predicts a power-supply and threshold voltages for high performance logic of about 0.9 V and 160 mV, respectively (in the later years). The targeted technology should have about the same values given that digital circuits are the main driving force in VLSI evolution and not to be optimized for analog circuits.

However, analog transistors do not need to have the shortest channel length possible. This is the reason why the transistors used in this work have 0.5 µm channel length. Using larger transistors also makes the process simulation task easier as patterns, by being much larger than the minimum feature sizes, minimize possible process simulator inaccuracies.

These simulators lay typically in TCAD frameworks and are capable of simulating the flow of single process steps to produce complete CMOS devices. Examples of TCAD frameworks come from both universities [8,9] and Electronic Design Automation (EDA) companies [10,11].

In this work the implemented technology used advanced features to control Short-Channel Effects, namely twin-tubes, halo implants, salicided gate-poly and trench

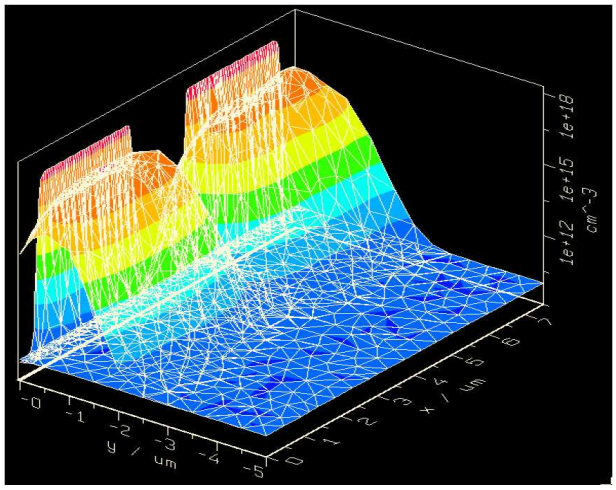

Fig. 2 - Profile of the net-doping after threshold adjustment implants (the simulation grid is also presented).

isolation. Fig. 2 displays the net-profile of a NMOS and a PMOS transistor that are aligned along the x-axis after applying the threshold adjustment implants. The simulators are also capable of calculating and refining the simulation grid, which is also present in the figure. A complete description of the process steps involved in the development of the final devices is beyond the scope of this paper. However a good description of the several process steps can be found in [12].

After process simulation the electrical parameters are obtained from device simulators. Several hundred simulations with MINIMOS [9] for many different bias conditions were performed to generate tables with drain current and terminal charges (see Fig. 3).

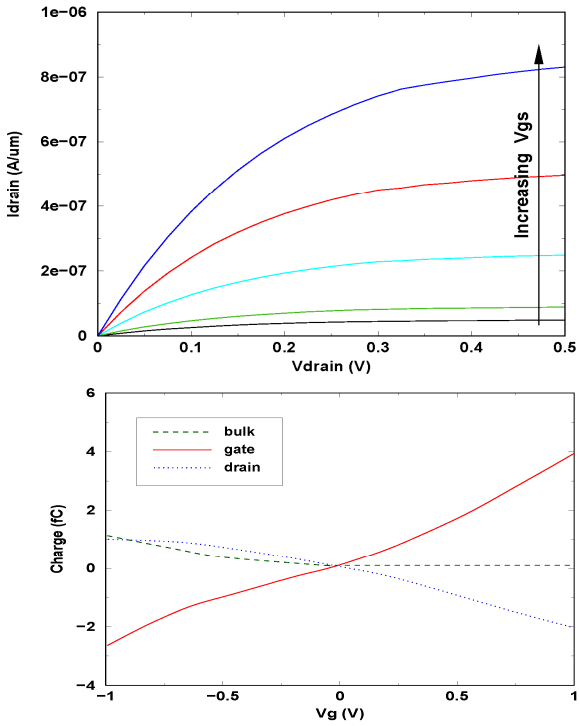

Fig. 3 - Top: drain current vs. drain-source voltage (at different V_{gs}); bottom: terminal charges vs. gate voltage.

TABLE I.
MOST IMPORTANT TRANSISTOR PARAMETERS (L= 0.5 μm).

	NMOS	PMOS
VDD	0.5 V	0.5 V
Vthreshold	0.25 V	0.25 V
Ion	17 μA	26 μA
Ioff	2.8 nA	1 nA

Bearing in mind the surmise that digital circuits are the main driving force of CMOS, the process was optimized primarily to give the highest Ion/Ioff current ratio. Other optimization objectives were equal threshold voltages and equal Ion currents for NMOS and PMOS transistors, as they are important to achieve the fastest switching speed. The device parameters obtained for 0.5 μm transistors are summarized in Table I.

Although symmetric threshold voltages were achieved, the equal drain currents objective was not. Nevertheless this is not a significant obstacle since large channel length (0.5 μm) transistors would not be used in logic circuits. Another consequence of large channel length is the increased threshold voltage. This is also acceptable as it causes lower power consumption due to reduced subthreshold leakage currents.

The operational amplifier circuit described in the next section was simulated with a table-driven circuit simulator that used data obtained from the device simulator. These data could also be used by parameter extraction tools for simulators that implement BSIM or EKV models. A 3D model of the interconnections was build to extract parasitic capacitances and wire resistances which were added to the circuit's netlist to precisely obtain bandwidth and stability results.

IV. CIRCUIT DESCRIPTION

This work aims for the design of an operational amplifier capable of working with power-supply voltage of only 0.5 V without using any special circuit techniques: e.g. in-chip voltage multiplication [13], floating-gate techniques [14] and threshold voltage tuning [15]. At such supply-voltage dynamic range is a principal concern and the use of rail to rail input and output stages is mandatory.

For ultra-low-power applications, the output should not by definition be too loaded, and therefore the input stage turns out to be the most difficult to design. A well known technique to achieve rail-to-rail operation is to place two complementary differential pairs in parallel (see Fig. 4). When the input common voltage approaches the negative rail, the PMOS transistors will be conveniently biased and the NMOS will be off. A complementary behavior is obtained when the input common mode voltage is approaching the positive rail. In the middle both differential pairs will be active and will contribute to the overall gain of the stage.

For typical circuits in strong inversion a power-supply voltage VDD-VSS greater than $2V_{th} + 2V_{DSsat}$ is necessary to proper operation (V_{th} is the threshold voltage and V_{DSsat} is the drain-source saturation voltage). However in low power technologies the concept of threshold voltage is not so precise. Indeed, in weak inversion transistors are biased at very low drain currents and saying that such transistor is on or off is not straightforward! Weak inversion is the key to reduce the supply voltage; for a drain current of 1 μA or less and a transistor width of 10 μm the gate-source voltage is smaller than the V_{th} reported in Table I.

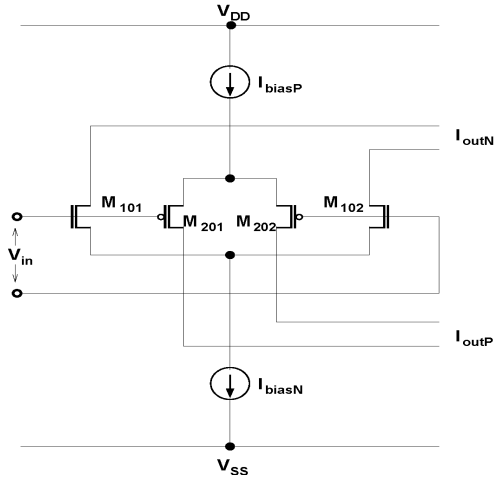

Fig. 4 - Rail-to-rail input stage.

A known problem of fixed biased complementary input stages is the change of the transconductance as the common mode input voltage varies, reaching a maximum when both pairs are active. However in weak inversion this problem can easily be overcome by keeping the sum of the tail currents constant (as the transconductance is proportional to the drain current).

For low-voltage circuits it is also important to avoid transistor stacking such as that found in cascode configurations. The circuit of Fig. 5 is also well balanced, an attractive feature to low-voltage operation (where good current mirrors are not available) even if the current consumption is slightly higher (there is one extra branch (transistors M106 and M107) wasting current (in comparison to a 2-stage Miller transconductor). It is to notice the possibility of connecting together the outputs of two of these circuits (one with a NMOS input and other with a PMOS input) effectively adding their transconductances. This can be seen in Fig. 6, presenting

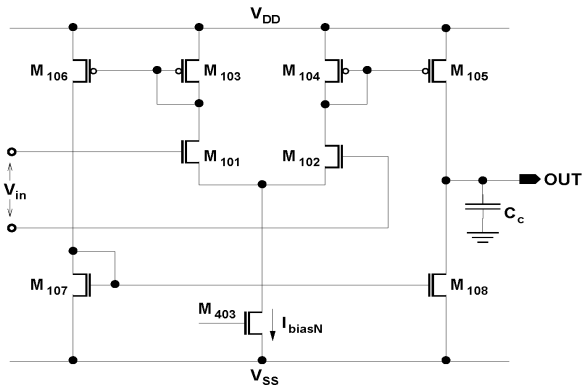

Fig. 5 - Balanced transconductor

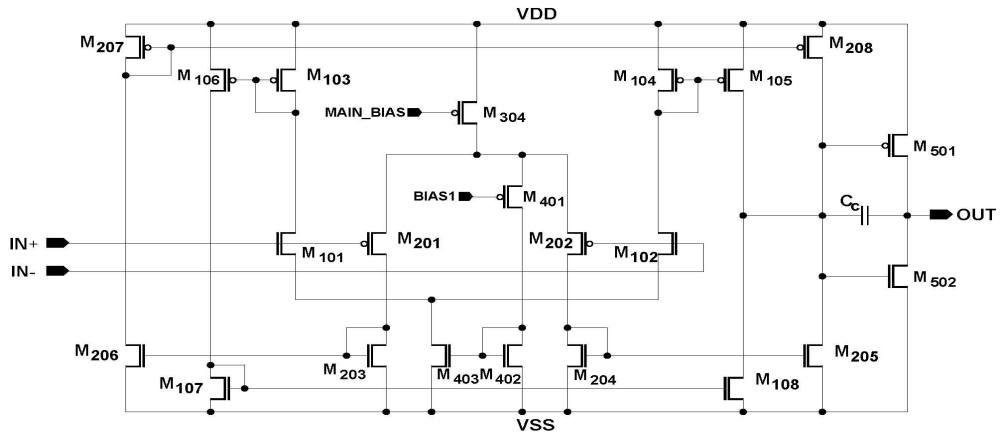

Fig. 6 - Complete schematic of the low-voltage, low-power operational amplifier.

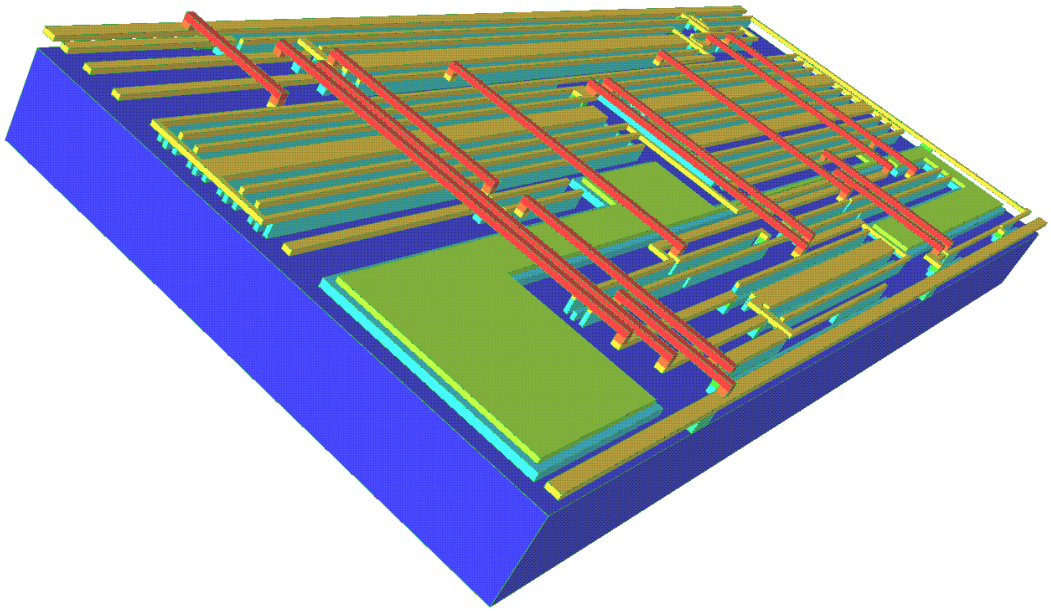

Fig. 7 – 3D model of the operational amplifier.

the complete schematic of the proposed operational amplifier. The constant total bias current function is performed by M401 and mirror M402-M403.

Fig. 6 also shows that the output stage is a simple inverter. This solution is simple, it is rail-to-rail and boosts the overall gain to more than 60 dB. The most serious disadvantage is the dependence on the drain current of M501 and M502 with the supply voltage. But for VDD-VSS less than 0.7 V this is not too much a problem.

To check the frequency response and stability problems, the 3D model of the opamp interconnections was build (fig. 7). After parasitics' extraction, it turned out that a 10 pF capacitor connected between the output and input of the output stage (named Cc in fig. 6) was needed to perform the frequency compensation. For higher gains Cc can obviously be reduced.

V. RESULTS AND CONCLUSIONS

Results presented here are obtained from circuit simulation of the circuit shown in Fig. 6. Regarding the first stage it turned out that the input transconductance changes ±5% with the input common mode voltage. This value is quite good and was confirmed with several transient simulations (like in Fig. 8) for all the input range that displayed similar overshoot/undershoot. Therefore the

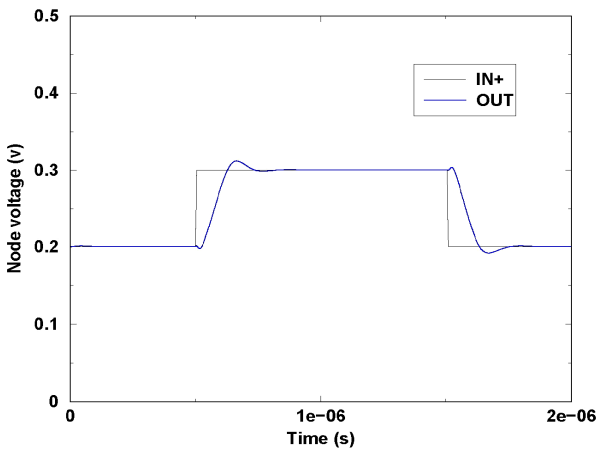

Fig. 8 - Transient response to a step (gain= 1 ; C_{Load}= 5 pF)

TABLE II.

MOST IMPORTANT OPAMP DATA (C_{LOAD}= 5 PF).

Parameter	Value
Power-supply voltage	0.5 V
Input and output swing	Rail-to-rail
Low frequency gain	64 dB
Unity-gain frequency	5 MHz
Slew-rate	0.9 V/µs
Total power comsumption	15 µW
Area	0.094 mm2

frequency stability is not changing with the input common mode voltage.

The simulations also demonstrated proper performance of the operational amplifier for supply voltages higher than 0.5 V. But above 0.7 V the bias current in the output transistors starts to increase, degrading the power efficiency of the amplifier; this could be solved with a more complex output stage. The gain also changes about 10% with VDD ranging from 0.5 V to 0.7 V, but an obtained minimum value of 64 dB is already enough for the majority of applications.

Table II resumes the most important results of the operational amplifier. It is to remark that the slew-rate is strongly dependant of the bias current and therefore can be traded with a power consumption penalty. However this trade is strongly limited in this design as the intput transistors should always stay in weak inversion.

These results presage good possibilities as regards the feasibility of designing ultra-low-voltage operational amplifiers in deep sub-micron technologies. To complete this work and be able to extend its forecast capabilities further in time, a similar study is required for UTB-FD and Dual Gate technologies.

VI. ACKNOWLEDGEMENT

This work was partially supported by Fundação para Ciência e Tecnologia – FCT, Portugal.

VII. REFERENCES

[1] E. S. Yang, Microelectronic Devices, Mc Graw Hill, 1988.

[2] R. Sarpeshkar, “Brain power,” Spectrum, pp.16–21, May 2006.

[3] G. E. Moore, “No exponential is forever: but “Forever” can be dealyed!,” 2003 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, vol. 1, pp. 20-23, Feb. 2003.

[4] W. Elgharbawi and M. Bayoumi, “Leakage sources and possible solutions in nanometer CMOS technologies,” IEEE Circuits and Systems Magazine, vol.5, Nbr. 4, pp.6-17, 2005.

[5] K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, and T. Cakici, “Double-gate SOI devices for low-power and high-performance applications,” in proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), San Jose, CA, pp. 217-224, Nov. 2005.

[6] Semiconductor Industry Association. The 2005 International Technology Roadmap for Semiconductors. San Jose, CA, 2005 http://www.itrs.net/Common/2005ITRS/Home2005.htm

[7] B.Calhoun, A. Wang, and A. Chandrakasan, “Modeling and sizing for minimum energy operation in subthreshold circuits,” IEEE J. Solid State Circuits, vol. 40, no.9, pp. 1778-1786, Sept. 2005.

[8] http//www-tcad.stanford.edu

[9] http://www.iue.tuwien.ac.at

[10] http://www.synopsis.com

[11] http://www.silvaco.com

[12] S. Wolf, The Submicron MOSFET, vol. 3 of Silicon Processing for the VLSI Era. Lattice Press, Sunset Beach, CA, 1995.

[13] T. Dusters and E. Dijkmans, “A -90 dB THD rail-to-rail input opamp using a new local charge pump in CMOS,” IEEE J. Solid State Circuits, vol. 33, no.7, pp. 947-55, July 1998.

[14] J. Ramírez-Angulo, A. López-Martín, and R. Carvajal, “Very low-voltage analog signal processing based on quasi-floating gate transistors”, IEEE J. Solid State Circuits, vol. 39, no.3, pp. 434-442, March 2004.

[15] Y. Tang and R. Geiger, “A 0.6 V ultra low voltage operational amplifier,” in Proc. IEEE International Symposeum on Circuits and Systems, Phoenix, AZ, May 2002.