Deterministic Wave and Random Symbol Phase Digital Synchronizers

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Resumo **- Neste artigo, apresentamos dois grupos de sincronizadores: o Sincronizador Digital pela Fase de Onda Deterministica e o Sincronizador Digital pela Fase de Símbolos Aleatórios.**

No primeiro caso, o VCO (Voltage Controlled Oscilator) sincroniza com a fase deterministica da onda regular de entrada e no segundo o VCO sincroniza com a fase aleatória da sequência de símbolos de entrada.

Em cada um destes grupos, apresentamos duas topologias digitais sendo a primeira do tipo combinacional e a segunda do tipo sequencial.

O nosso principal objectivo é estudar os dois grupos, o deterministico e o aleatório, nas suas duas tipologias combinacional e sequencial e observar o seu comportamento de jitter em função do ruído.

Palavras chave: **Sincronismo em Comunicações Digitais**

Abstract **- In this paper, we present two groups of synchronizers: the Deterministic Wave Phase Digital Synchronizer and the Random Symbol Phase Digital Synchronizer.**

In the first case, the VCO (Voltage Controlled Oscillator) synchronizes with the deterministic phase of the input regular wave and in the second the VCO synchronizes with the random phase of the input random symbols.

In each one of this groups, we present two digital topologies being the first one the combinational type and the second the sequential type.

Our main objective is to study the two deterministic and random groups in its two combinational and sequential typologies and to observe its jitter behavior as function of the noise.

Key words: **Synchronism in Digital Communications**

I. INTRODUCTION

This work deal with two synchronizer groups, in the first, the synchronizer VCO (Voltage Controlled Oscillator) synchronizes with the deterministic phase of a regular wave and in the second, the synchronizer VCO synchronizes with the random phase of a symbol sequence.

Each group has two digital prototypes being one of combinational type and the other of sequential type.

The digital synchronizer of combinational type is composed only by combinational logic gates, then is known as a circuit without intern memory. Whereas, the digital synchronizer of sequential type is composed by logic gates and flip flops, then is known as a circuit with intern memory.

Then, our interest is to observe as the memory affects the behavior of each synchronizer in the presence of the noise.

Basically, a synchronizer is a device based on a VCO, which is able to follow the phase of an input signal. This means that the VCO output is synchronous with the input signal.

Following figure (Fig.1) shows the block diagram of a general synchronizer.

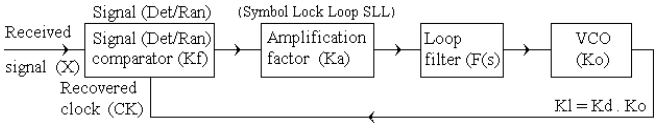

Fig.1 General deterministic or random synchronizer

F(s) is the loop filter, Ko is the VCO gain, Kf is the signal comparator gain and Ka is the parameter of the loop gain that acts in the locus root getting the desired characteristics.

Next, we present the two deterministic and random synchronizer groups, each one with its two digital prototypes: the combinational and the sequential.

After, we test all the synchronizers with a signal corrupt by noise.

Later, we present the results and we make some comparisons,

Finally, we present the main conclusions.

II. DETERMINISTIC PHASE SYNCHRONIZERS

In this group of phase digital synchronizers, we present two digital topologies: the combinational type and the sequential type [1, 2].

Following figure (Fig.2) shows the combinational type that is composed by logic gates.

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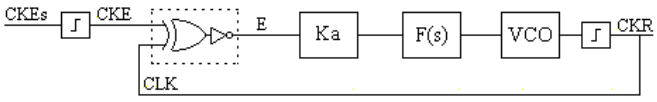

Fig.2 Combinational phase digital synchronizer

The signal or deterministic phase comparator is of combinational type since it is based on an exor gate. So it provides the combinational phase digial synchronizer.

The exor gate is a component without memory, then the respective phase synchronizer is a device without intern memory.

Following figure (Fig.3) shows the sequential type, which is composed by a flip flop and additional logic gates.

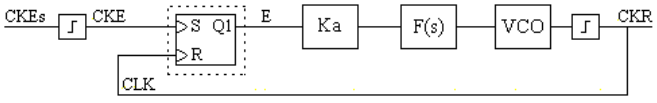

Fig.3 Sequential phase digital synchronizer

The deterministic phase comparator is of sequential type since it is based on a flip flop. So it provides the sequential phase digital synchronizer.

The flip flop is a component with memory, then the respective phase synchronizer is a device with intern memory.

III. RANDOM PHASE SYNCHRONIZERS

In this group of symbol digital synchronizers, we present two digital topologies: the combinational type and the sequential type [3, 4].

The following figure (Fig.4) shows the combinational symbol digital synchronizer which is composed by logic gates.

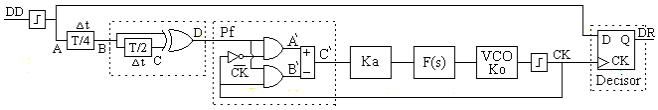

Fig.4 Combinational symbol digital synchronizer

The signal or random phase comparator is of combinational type since it is based on an exor and AND gates. So it provides the combinational symbol digital synchronizer.

The exor gates are components without memory, then the respective symbol synchronizer is a device without intern memory.

The following figure (Fig.5) shows the sequential type which is composed by flip flops and additional logic gates.

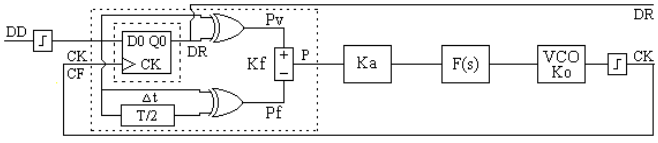

Fig.5 Sequential sylbol digital synchronizer

The random phase comparator is of sequential type since it is based on flip flops. So it provides the sequential symbol digital synchronizer.

The flip flops are components with memory, then the respective symbol synchronizer is a device with intern memory.

IV. TESTS, DESIGN AND RESULTS

We present the tests, the design and the results of the refereed synchronizers [5].

A. Tests

The following figure (Fig.6) shows the setup that was used to test the various synchronizers.

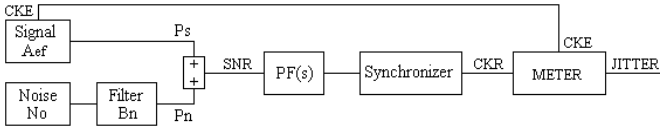

Fig.6 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

B. Jitter measurer

The jitter measurer (Meter) consists of a RS flip flop which detects the random variable phase of the recovered clock (CKR) relatively to the fixed phase of the emitter clock (CKE).

This relative random phase variation is the recovered clock jitter (Fig.7).

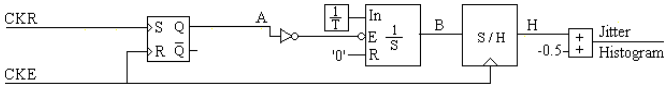

Fig.7 The jitter measurer (Meter)

The others blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

C. Design

To have guaranteed results it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud what implies also normalized values for the others

dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalized this values to the appropriated transmission rate tx.

Now, we will apply a signal to noise ratio SNR related with the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn it is SNR = $A^2_{ef}/(No.Bn)$. But No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the combinational synchronizers, the bandwidth is

$$Bl=0.02=(KaKfKo)/4$$
$$Kf=1/\pi; Ko=2\pi; Ka=0.04 \quad (3)$$

For the sequential synchronizers, the bandwidth is

$$Bl=0.02=(KaKfKo)/4$$
$$Kf=(1/2\pi); Ko=2\pi; Ka=0.08 \quad (4)$$

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For analog PLL the jitter is

$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau=0.02*10^{-3}*2\sigma n^2/0.5^2=16*10^{-5}.\sigma n^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not considered here, but the results are similar with the ones obtained above.

D. Results

We present the results of the two groups of synchronizers: the deterministic and the random. In each group we distinguish the combinational and the sequential types.

We can see the jitter as function of the SNR (Signal to noise ratio).

Initially, we present the jitter-SNR curves of the two deterministic wave synchronizers: the combinational type (cmb) and the sequential type (seq) (Fig.8).

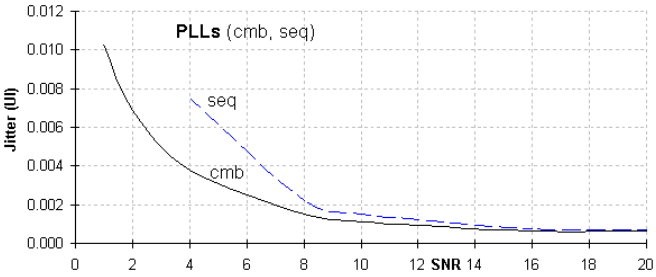

Fig.8 Jitter-SNR curves of the two wave synchronizers (c, s)

We verify, that for high SNR, the two synchronizers (cmb, seq) have similar performance. However, for low SNR the combinational type has a slightly advantage.

After, we present the jitter-SNR curves of the two random symbol digital synchronizers: the combinational type (cmb) and the sequential type (seq) (Fig.9).

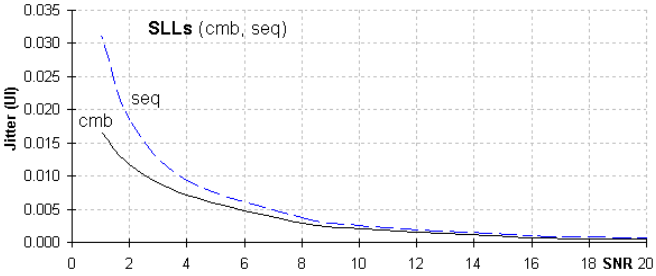

Fig.9 Jitter-SNR curves of the two symbol synchronizers (c, s)

We verify that for high SNR the two synchronizers (cmb, seq) have similar performance. However, for low SNR the combinational type has a slightly advantage.

V. CONCLUSIONS

We studied two synchronizer groups, which are the deterministic wave phase digital synchronizers and the random symbol phase digital synchronizers. Each group has two types: the combinational (cmb) and the sequential (seq).

In both groups, for high SNR the combinational and sequential types have similar jitter-SNR performance. However, for low SNR the combinational type has a slightly advantage over the sequential.

This behavior is comprehensible, for high SNR, due to the noise margin of the digital components in which little noise spikes are ignored. However, for low SNR, the big noise spikes cause random state transitions, which increases slightly the jitter of the sequential type. Anyway, this last disadvantage can be minimized with a prefilter.

The sequential type has particular potentialities, due to its comparator memory, to operation at different frequencies of the transmission rate and permits automatic versions.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

[1] A. H. Jazwinski, "Filtering for Nonlinear Dynamical Systems" IEEE Automatic Control p.765 October 1966.

[2] J. C. Imbeaux, "performance of the delay-line multiplier circuit for clock and carrier synchronization", IEEE, J. Sel. Areas in Com., Jan. 1983.

[3] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Transactions on Communications com-30. October 1982.

[4] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", Journal of Lightwave Technology, Dec. 1985.

[5] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "A New Technique to Measure the Jitter", III Conference on Telecommunications p.64, F. Foz-PT 23-24 April 2001.