Sequential Synchronizers with the Pulse Comparation and Clock Sampling Variants

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Resumo **- A função do sincronizador é amostrar os dados com a minima taxa de erros (BER) e retemporizar a duração dos seus bits com o formato original.**

Neste trabalho, apresentamos o sincronizador sequencial com duas variantes que são a de comparação de pulsos criado por Hogge e a de amostragem de relógio criada por nós. Cada variante tem duas versões que são a manual e a automática.

O principal objectivo é estudar, nos quatro sincronizadores, o jitter de saída como função da relação sinal-ruído de entrada.

Abstract **- The function of the synchronizer is to sample the data with the minimum bit error rate (BER) and to retime its bit duration with the original format.**

In this work, we present the sequential synchronizer with two variants which are the pulse comparation discovered by Hogge and the clock sampling discovered by us. Each variant has two versions which are the manual and the automatic.

The main objective is to study, in the four synchronizers, the output jitter as function of the input signal-to-noise ratio.

I. INTRODUCTION

The conventional PLL (Phase Lock Loop) synchronizes its VCO (Voltage Controlled Oscillator) with the input carrier wave (deterministic regular signal). Then we have the WPLL (Wave Phase Lock Loop).

The special PLL is able to synchronize its VCO with the input bit/symbol string of data sequence (random irregular signal). Then we have the SPLL (Symbol Phase Lock Loop) or BPLL (Bit Phase Lock Loop), we prefer the first designation to avoid confusion with the Block Synchronizer.

The PLL can still synchronize its VCO with the block of data sequence as happen with the synthesizer of the block codes mBnB. Then we have the BPLL (Block Phase Lock Loop). This BPLL can receive an input data rate and transmit a different output data rate.

In this work, we center the study only in the symbol synchronizer (SPLL). In the SPLL there are four types which are the analog, hybrid, combinational and sequential.

Here, we take the sequential synchronizer considering two variants, which are the pulse comparation discovered by Hogge and the clock sampling discovered by us. Each variant has two versions: the manual and the automatic.

Following Fig.1 shows the general configuration of the symbol synchronizer.

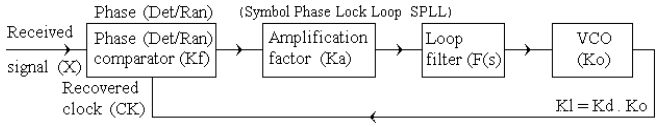

Fig.1 General configuration of the symbol synchronizer

F(s) is the loop filter, Ko is the VCO gain, Kf is the signal comparator gain and Ka is the parameter of the loop gain that acts in the locus root getting the desired characteristics.

First, we show the function of the symbol synchronizer.

Next, we present the two sequences generators used to test the four synchronizers.

After, we present the basic principles of the each synchronizer variant.

Later, we show each synchronizer variant with their two manual and automatic versions.

Following, we design and test all the synchronizers with a signal corrupted by noise.

Then, we present the results with some comparisons.

II. THE FUNCTION OF THE SYNCHRONIZER

The symbol synchronizer recoveries the clock that is a regular wave at the bit rate. The clock can also be used by others blocks of the link [1, 2, 3, 4, 5, 6, 7].

The main functions of the symbol synchronizer is to sample the data with the minimum bit error rate (Fig.2a) and to retime the bit duration with the original format (Fig2b).

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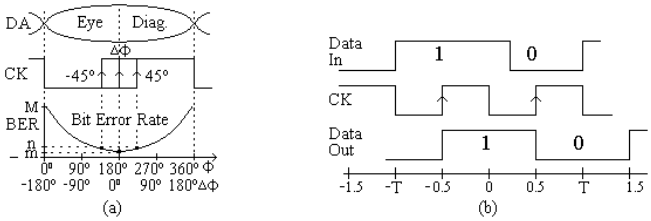

Fig.2 Data sampling (a) and data retiming (b)

The input data must be sampled at maximum eye diagram in order to minimize the bit error rate. The output data, previously, must be retimed in order to reach the original bit duration.

III. TWO SEQUENCES FOR TEST

Following Fig.3 shows the two sequence generators that produces the two sequences to test the four symbol synchronizers [8, 9, 10, 11, 12]

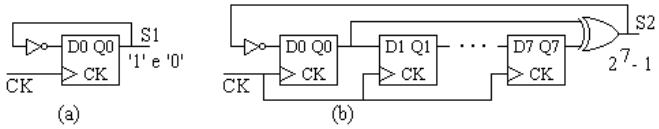

Fig.3 Sequences: S1= alternated 1and 0 (a) and S2= PR 2^7-1(b)

The left generator produces the alternated (A) '1' and '0' sequence S1 of length 2 and the right generator produces the pseudo- random (PR) sequence S2 of length 2^7-1.

IV.TWO VARIANTS OF SEQUENTIAL SYMBOL SYNCHRONIZERS

We will present the sequential symbol synchronizer with the basic principles of the two referred variants [13, 14, 15].

The pulse comparation variant, proposed by Hogge, is based on the comparation between a variable pulse Pv with a fixed pulse Pf, determining the error pulse direction Pr.

The clock sampling variant, proposed by us, is based on the sampling of the clock by the input data transition, determining the load pulse direction P (Fig.4).

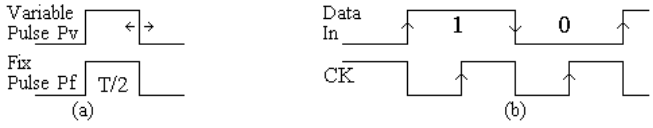

Fig.4 Variants of pulse comparation(a) and clock sampling (b)

Following, we will present the two synchronizer variants each with their two versions the manual and the automatic.

V. VARIANT OF PULSE COMPARATION

The pulse comparation variant, proposed by Hogge, is based on the comparation between a variable pulse Pv with a fixed pulse Pf, resulting an error pulse Pr. At the equilibrium point the two pulses are equal, then the error pulse is null. When the clock delay, the error pulse is positive that increases the clock frequency advancing its phase. When the clock advances, the error pulse is negative that decreases the clock frequency delaying its phase [4].

For this variant we consider two versions which are the manual and the automatic. The variable pulse Pv is similar in the two versions, the difference is in the fixed pulse Pf.

The variable pulse Pv is produced between each input data transition and the clock positive transition.

Following Fig.5 shows the manual version, in which the fixed pulse is produced by previous adjust of a delay line.

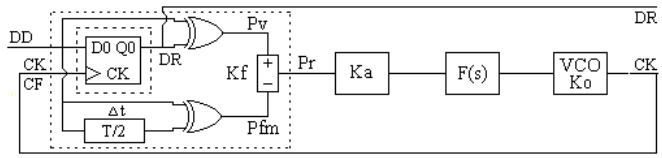

Fig.5 Pulse comparation variant and manual version (pcm)

The fixed pulse Pf is produced between each direct data transition and the delayed data transition in a delay line (T/2) previously adjusted and an exor.

Following Fig.6 shows the automatic version, in which the fixed pulse is automatically produced by the 2nd flip flop.

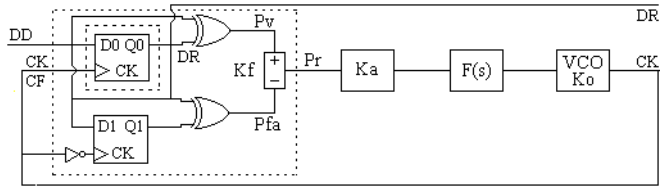

Fig.6 Pulse comparation variant and automatic version (CPa)

The fixed pulse Pfa is produced automatically with the help of the clock, the second flip flop and exor. After each data transitions between the clock positive transition and the clock negative transition is produced the fixed pulse Pfa with duration of T/2.

VI. VARIANT OF CLOCK SAMPLING

The clock sampling variant, proposed by us, is based on the sampling of the clock by the input transition data. At the equilibrium point the negative clock transition is coincident with the data transition and no correction is needed. When the clock delay an error positive pulse P increases the clock frequency advancing its phase. When the clock advances an error negative pulse P decreases the clock frequency delaying its phase [5].

For this variant we consider two versions which are the manual and the automatic. In both versions, the first flip flop triggered by the data, samples the clock. The difference is in the mode as is created the load pulse of the filter. A great advantage is that this pulse fixed duration (T/2) is not critic.

Following Fig.7 shows the manual version, in which the load pulse is produced by previous adjust of a delay line.

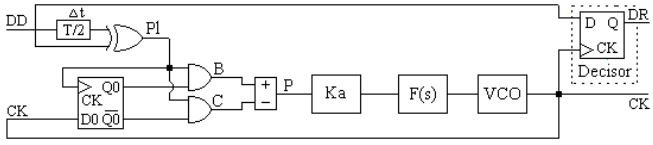

Fig.7 Clock sampling variant and manual version (ARm)

In this version, the fixed load pulse Pl is produced by a non critic previous adjust delay line of T/2 and an exor.

Following Fig.8 shows the automatic version, in which the load pulse is produced automatically by the second flip flop.

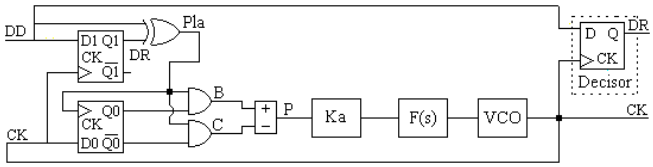

Fig.8 Clock sampling variant and automatic version (ARa)

In this version, the variable load pulse Pla is produced automatically by the second flip flop and exor.

VII. DESIGN, TESTS AND RESULTS

We present the design, the tests and the results of the refereed synchronizers [5].

A. Design

To have guaranteed results it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer characteristic functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalized this values to the appropriated transmission rate tx.

Now, we will apply a signal to noise ratio SNR related with the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn it is SNR = $A^2_{ef}/(No.Bn)$. But No can be related with the noise variance σn and inverse sampling $\Delta\tau=1/Samp$, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{\mathrm{G(s)}}{1+\mathrm{G(s)}}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$\mathrm{Bl}=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is Bl = 0.02 = (Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=1/2; Ko=2π)

$$(Ka.Km.A.B.Ko)/4 = 0.02\mathtt{i}\ Ka = 0.08\times 2/\pi \quad (3)$$

For the hybrid synchronizers, the loop bandwidth is Bl = 0.02 = (Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=0.45; Ko=2π)

$$(Ka.Km.A.B.Ko)/4 = 0.02\ \mathtt{i}\ Ka = 0.08\times 2.2/\pi \quad (4)$$

For the combinational synchronizers, the bandwidth is Bl = 0.02 = (Ka.Kf.Ko)/4 with (Kf = 1/π; Ko = 2π)

$$(Ka\times 1/\pi\times 2\pi)/4 = 0.02\ \mathtt{i}\ Ka = 0.04 \quad (5)$$

For the sequential synchronizers, the bandwidth is Bl = 0.02 = (Ka.Kf.Ko)/4 with (Kf = 1/2π; Ko = 2π)

$$(Ka\times 1/2\pi\times 2\pi)/4 = 0.02\mathtt{i}\ Ka = 0.08 \quad (6)$$

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For analog PLL the jitter is

$$\sigma^2_\phi = B1.No/Aef^2 = B1.2\sigma^2_n.\Delta\tau = 0.02\times 2\sigma^2_n/0.5^2 = 16\times 10^{-5}\sigma^2_n \quad (7)$$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not considered here, but the results are similar with the ones obtained above.

B. Tests

Following Fig.9 shows the setup that was used to test the various synchronizers.

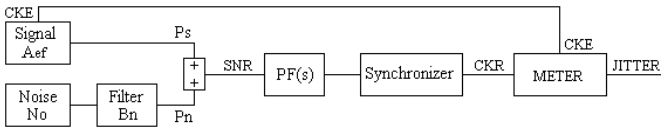

Fig.9 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer

The jitter measurer (Meter) consists of a RS flip flop which detects the random variable phase of the recovered clock (CKR) relatively to the fixed phase of the emitter clock (CKE).

This relative random phase variation is the recovered clock jitter (Fig.10).

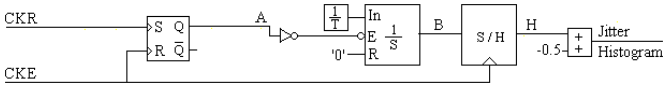

Fig.10 The jitter measurer (Meter)

The others blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We present the output jitter-input SNR curves of the four synchronizers tested firstly with the sequence S1 of '1' and '0' alternated and after with the sequence S2 pseudo-random of length 2^7-1.

Following Fig.8 shows the jitter-SNR curves of the four synchronizers namely the pulse comparation manual version (pcm1), pulse comparation automatic version (pca1), clock sampling manual version (csm1), clock sampling automatic version (csa1) with sequence S1.

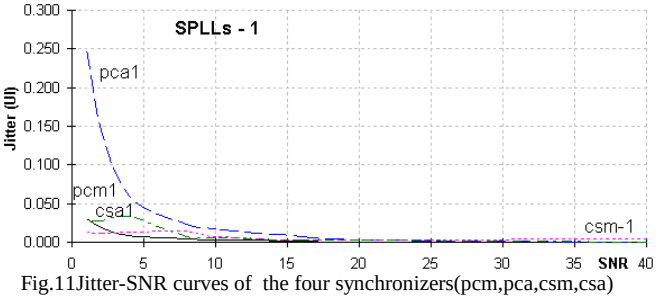

Fig.11Jitter-SNR curves of the four synchronizers(pcm,pca,csm,csa)

We verify, that for high SNR, the four synchronizers have similar performance. However, for low SNR the pulse comparation manual version is preferable.

Following Fig.12 shows the jitter-SNR curves of the synchronizers pulse comparation manual (pcm7), pulse comparation automatic (pca7), clock sampling manual (csm7), clock sampling automatic (csa7) with sequence S2.

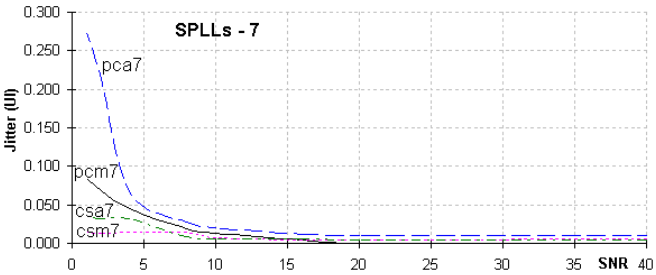

Fig.12Jitter-SNR curves of the four synchronizers(pcm,pca,csm,csa)

We verify, that for high SNR, the four synchronizers are similar. However, for low SNR the pulse comparation manual has a slightly advantage. The pulse comparation is more sensible to the sequence type than the clock sampling.

VIII. CONCLUSIONS

We studied two synchronizers variants which are the pulse comparation and the clock sampling. Each variant has two versions which are the manual and the automatic.

We studied the jitter-SNR curves of the four synchronizers tested firstly with a sequence S1 of '1' and '0' alternated and after with a sequence pseudo-random S2 of length 2^7-1.

The discrete operation of the clock sampling variant produces an insignificant disturbance although the continuous operation of the pulse comparation variant produces null disturbance. So, the total disturbance is due only to the noise.

With the two sequences S1 and S2, for high SNR (SNR>8) the four synchronizers are similar. Then, we can use anyone, but due to its simplicity the clock sampling automatic version is preferable. However, for low SNR (SNR<8) the clock sampling versions have synchronism problems and the pulse comparation automatic version has more jitter. Then we must use the pulse comparation manual version.

The pulse comparation is more sensible with the sequence type, than the clock sampling that is almost insensible.

ACKNOWLEDGMENTS

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