Four Symbol Phase Synchronizers Tested with Three Input Sequences

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Resumo **- Este trabalho estuda quatro sincronizadores de símbolo, nomeadamente o analógico, o hibrido, o combinacional e o sequencial.**

Estes quatro sincronizadores serão testados com três diferentes sequências de entrada (P1, P2 e P7). P1=2^1 (1um-1zero 1-0) é deterministica, P2=2^2 (2uns-2zeros 11-00) é deterministica e P7=2^7-1 (1.....0) é pseudo-aleatória.

O objectivo é estudar os quatro sincronizadores e avaliar os seus jitter UI-RMS (Unidades Intervalo -Valor efectivo) em função da entrada SNR (Relação Sinal Ruído), quando a entrada varia entre P1, P2 e P7.

Abstract **- This work study four symbol synchronizers namely the analog, hybrid, combinational and sequential.**

These four synchronizers will be tested with three different input sequences (P1, P2 and P7). P1=2^1 (1one-1zero 1-0) is deterministic, P2=2^2 (2ones-2zeros 11-00) is deterministic and P7=2^7-1 (1 ... 0) is pseudo - random.

The objective is to study the four synchronizers and to evaluate their jitter UI-RMS (Unit Interval-Root Mean Squared) versus input SNR (Signal- Noise Ratio), when the input sequence changes between P1, P2 and P7.

I. INTRODUCTION

The symbol synchronizer is a subsystem that recoveries the data, sampling the symbols with the minimum bit error rate and retimes its duration to the original format. The synchronizer has a VCO (Voltage Controlled Oscillator) that is able to follow the input sequence transitions [1, 2, 3, 4, 5].

This work study four symbol synchronizers namely the analog, hybrid, combinational and sequential. The difference of them is in the phase comparator/detector [6, 7, 8, 9, 10].

The four synchronizers will be tested with three input sequences P1, P2 and P7. P1 is deterministic, consists of one and zero alternated (1-0), P2 is deterministic consisting of two ones and two zeros alternated (11-00) and P7 is pseudo-random consisting of a length 2^7-1 (1...0) [11, 12, 13].

Fig.1 shows the general aspect of the symbol synchronizer.

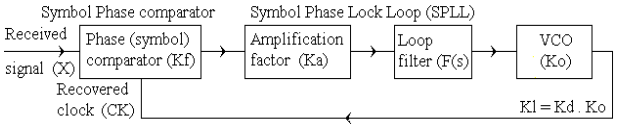


Fig.1 General blocks diagram of the symbol phase synchronizer

Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop gain that controls the root locus and therefore the loop characteristics.

Following, we will present the four symbol synchronizers namely the analog, hybrid, combinational and sequential.

Next, we show the three input sequences of test, with formats P1=2^1, P2=2^2 and P7=2^7-1.

After, we will present the design and the tests of the synchronizers jitter in the presence of noise.

Then, we present the results, based on jitter-SNR curves.

Finally, we present the conclusions.

II. THE FOUR SYMBOL PHASE SYNCHRONIZERS

We present four symbol phase synchronizers, namely the analog, hybrid, combinational and sequential. The difference between them is only in the symbol phase comparator / detector [3, 4].

A. Analog type

Fig.2 shows the analog type, its phase comparator is based on the analog ideal switches.

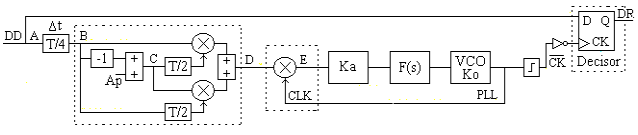


Fig.2 Analog symbol phase synchronizer

The two inputs (main input and VCO output) of the symbol phase comparator are both analog (full-analog).

B. Hybrid type

Fig.3 shows the hybrid type, its phase comparator is based on the hybrid real switch.

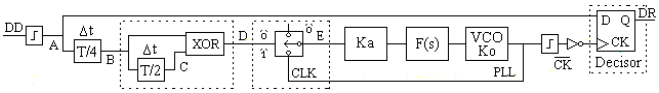


Fig.3 Hybrid symbol phase synchronizer

The two inputs (main input and VCO output) of the symbol phase comparator is the first digital and the second is still analog (half-analog).

C. Combinational type

Fig.4 shows the combinational type, its phase comparator is based on an exor gate.

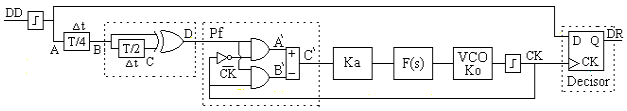


Fig.4 Combinational symbol phase synchronizer

The two inputs (main input and VCO output) of the symbol phase comparator are both digital (digital-combinational). The output is only function of the inputs (circuit without memory).

D. Sequential type

Fig.5 shows the sequential type, its phase comparator is based on a flip flop and additional logic gates.

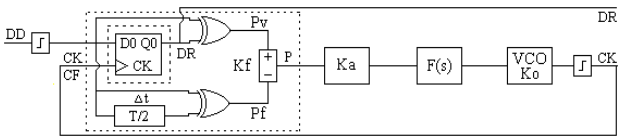


Fig.5 Sequential symbol phase synchronizer

The two inputs (main input and VCO output) of the symbol phase comparator are both digital (digital-sequential). The output is simultaneously function of the inputs and the state (circuit with memory).

III.THE INPUT SEQUENCES OF TEST

We use the following generators to produce the three different input sequences P1, P2 and P7 (Fig.6).

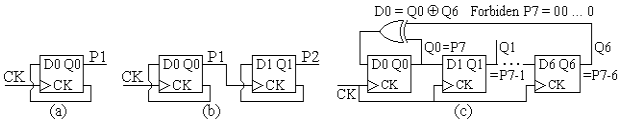


Fig.6 The three sequence generators: $P1=2^1$, $P2=2^2$ and $P7=2^7-1$

P1 and P2 are based on flip flops but P7 is based on a shift register with appropriate feedback to provide maximum length sequences MLS [3, 4].

Tab.1 shows the basic principles of sequences P1, P2, P7.

Tab.1 - The three sequences configuration

Determini.	P. Random	Length	Feedback
D '1'- '0' P1= 2^1	---	P1= 2^1 = 2	(a) ---
D'11'- '00' P2 = 2^2	---	P2= 2^2 = 4	(b) ---
---	PR P7 = 2^7-1	P7=2^7-1 =127	(c) D0=Q0⊕Q6

P1 is a deterministic sequence with length 2 (1-0) and has x data transitions.

P2 is a deterministic sequence with length 4 (11-00) and has x/2 data transitions.

P7 is a pseudo-random sequence with length 2^7-1 (1 ... 0) and has x/2 data transitions.

We used also pseudo random sequences of length P15= 2^{15}-1 and P23=2^{23}-1. But the results are equal to P7=2^7-1.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [6].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can resclae these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling Δτ=1/Samp, then No=$2\sigma n^2.\Delta\tau$, so SNR=$A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{G(s)}{1+G(s)}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=1/2; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi$ (3)

For the hybrid synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Km=1, A=1/2, B=0.45; Ko=2π)

$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi$ (4)

For the combinational synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/π; Ko=2π)

$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5)

For the sequential synchronizers, the loop bandwidth is

$Bl=0.02=(Ka.Kf.Ko)/4$ with (Kf=1/2π; Ko=2π)

$(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl.

For the analog PLL the jitter is

$\sigma\phi^2=Bl.No/Aef^2=Bl.2.\sigma n^2.\Delta\tau/Aef^2=0.02*2\sigma n^2*10^{-3}/0.5^2$

$=16*10^{-5}.\sigma n^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

Fig.7 shows the setup that was used to test the various synchronizers.

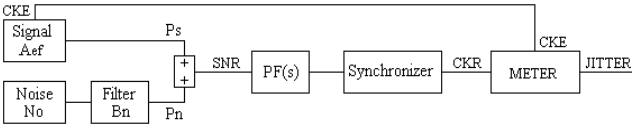


Fig.7 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.8).

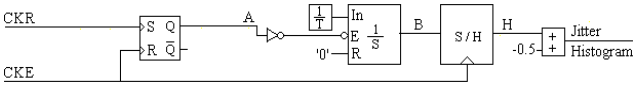


Fig.8 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present separately the jitter-noise curves of the four symbol synchronizers for the three input sequences.

Fig.9 shows the UI-RMS jitter - SNR curves of the four synchronizers (ana, hib, cmb, seq) for the input deterministic sequence P1 (1one-1zero).

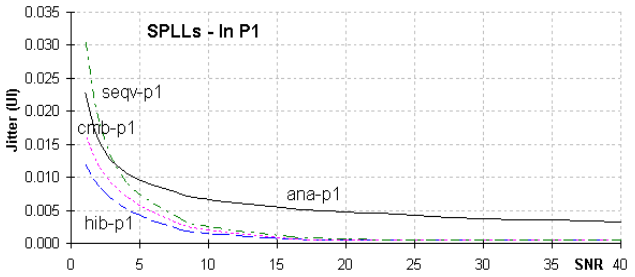


Fig.9 Jitter-SNR curves of the four synchronizers with (in P1)

We verify, that for high SNR the synchronizer without input limiter (ana) has the worst performance and the synchronizers with input limiter (hib, cmb, seq) are similar.

For low SNR the sequential synchronizer (with intern memory) has slightly the worst performance.

Fig.10 shows the UI-RMS jitter - SNR curves of the four synchronizers (ana, hib, cmb, seq) for the input deterministic sequence P2 (2ones-2zeros).

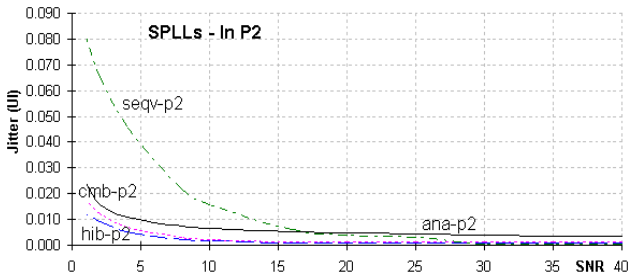
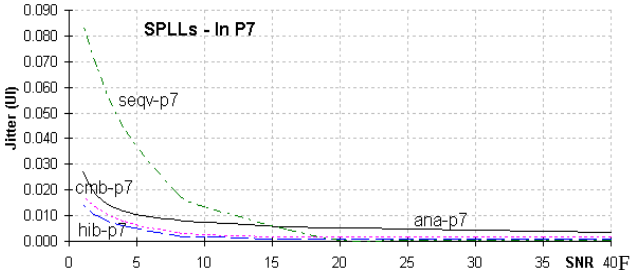


Fig.10 Jitter-SNR curves of the four synchronizers with (in P2)

We verify, that for high SNR the synchronizer without input limiter (ana) has the worst performance and the synchronizers with input limiter (hib, cmb, seq) are similar.

For low SNR the sequential synchronizer (with intern memory) has significantly the worst performance.

Fig.11 shows the UI-RMS jitter - SNR curves of the four synchronizers (ana, hib, cmb, seq) for the input pseudo-random sequence P7 (2^7-1).



ig.11 Jitter-SNR curves of the four synchronizers with (in P7)

We verify, that for high SNR the synchronizer without input limiter (ana) has the worst performance and the synchronizers with input limiter (hib, cmb, seq) are similar.

For low SNR the sequential synchronizer (with intern memory) has significantly the worst performance.

V. CONCLUSIONS

We studied four symbol synchronizers namely the analog, the hybrid, the combinational and the sequential. Then we tested their jitter versus input SNR, with three different input sequences P1 (deterministic one-zero with x data transitions, P2 (deterministic 2ones-2zeros with x/2 data transitions) and P7 (pseudo-random 2^7-1 with x/2 data transitions).

We observed that generally, the output jitter decreases almost exponentially when the input SNR increases.

For the sequence P1 (one-zero - x transitions), we noted that for high SNR, the synchronizer without input limiter (ana) has the worst performance and the synchronizers with input limiter (hib, cmb, seq) are similar. This is comprehensible since the limiter noise margin ignores low noise spikes, what decreases the jitter. For low SNR, the sequential synchronizer (with intern memory) has slightly the worst performance. This is comprehensible since the noise spikes provokes random gate commutations what increases the jitter.

For the sequences P2 (2ones-2zeros - x/2 transitions) and P7 (27-1 - x/2 transitions) the synchronizers without intern memory (ana, hib, cmb) have similar behavior. However the synchronizer with intern memory (seq) degrades its behavior when the sequence diminishes the number of transitions P1 -> (P2, P7). This is comprehensible since when the noise spike conducts to the error state, this situation only is corrected in the next data transition then P1 (with x transitions) corrects the situation more quickly than P2 or P7 (with x/2 data transitions).

ACKNOWLEDGMENTS

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