Impact of the Noise Spikes on Sequential Symbol Synchronizers

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Resumo **- Este trabalho estuda o impacto dos picos de ruído nos sincronizadores de símbolo sequencial.**

Distinguimos duas variantes de sincronizadores que são: a que processa ambas as transições de dados e a que processa apenas a transição positiva dos dados. Em cada uma, consideramos duas versões nomeadamente a manual e a automática.

O objectivo é estudar, nos vários sincronizadores, a saída de jitter UIRMS (Unidades Intervalo da Raíz Média Quadrática) versus a entrada SNR (Relação Sinal Ruído).

Palavras chave: Sincronismo em Sistems de Comunicações

Abstract **- This work study the impact of the noise spikes on sequential symbol synchronizers.**

We distinguish two synchronizers variants which are: the one that processes the both data transitions and the one that process only the positive data transition. In each one, we consider two versions namely the manual and the automatic.

The objective is to study the various synchronizers output jitter UIRMS (Unit Interval Root Mean Square) versus the input SNR (Signal to Noise Ratio).

I. INTRODUCTION

This work study the impact of the noise spikes on sequential symbol synchronizers.

The sequential symbol synchronizer has a phase detector with intern memory, then the output depends of the input and also of the state [1, 2, 3, 4, 5].

So, the noise spikes conduct to the error state and this contributes also to the output jitter increasing [6, 7, 8, 9, 10].

To understand the issue, we present two variants, namely the both data transitions and the positive data transition. In each variant, we consider the manual version and the automatic version [11, 12, 13].

Fig.1 illustrate as the noise spikes conducts the system to the error state, what increases the output jitter.

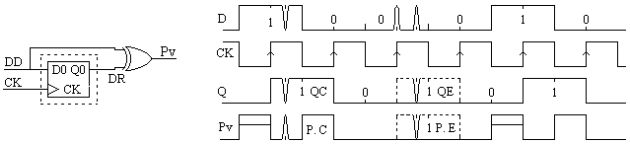

Fig.1 Contribution of the error state to the jitter increasing

The output Pv with jitter depends of the input D (signal corrupted by noise) and also of the flip flop state Q that can be correct QC or erroneous QE. So, the erroneous state QE contributes extensively to the output jitter.

The variable pulse Pv must be compared with the reference pulse Pf that correspond to the equilibrium point.

The width of pulse Pf determines the width of Pv at the equilibrium point, that corresponds to the correct sampling.

The waveforms show the input signal to be processed normally in the correct state QC and only during one period T to be processed in the error state QE.

Following, we present the variant of both data transitions with its versions manual and automatic.

Next, we present the variant of positive data transition with its versions manual and automatic.

After, we present the design and tests.

Then, we present the results.

Finally, we present the conclusions.

II. BOTH TRANSITIONS SYNCHRONIZERS

The synchronizers of both data transitions uses the synchronism information of both data transitions (positive and negative). These synchronizers make a pulse comparation (variable pulse Pv and fixe pulse Pf) in all the data transitions [5].

A. Both transitions synchronizers - manual

This synchronizer uses both data transitions and the fixed pulse Pf is produced with previous manual adjusting of the delay $\Delta t=T/2$ (Fig.2).

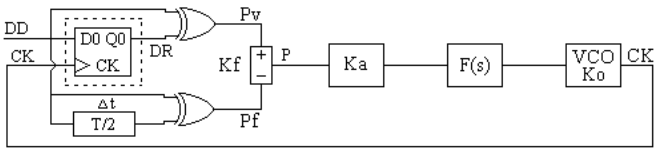

Fig.2 Manual both transitions synchronizer (seqv-m)

The phase comparator inputs (input and VCO) are both digital. The output is function of the input and state.

Following figure shows the waveforms that illustrate the operation mode of this synchronizer (Fig.3).

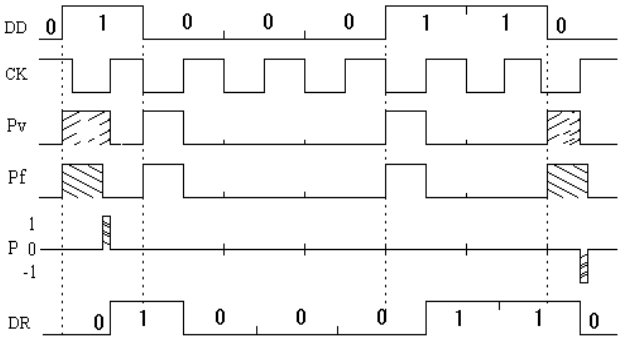

Fig.3 Waveforms of the manual both transitions (seqv-m)

The variable pulse Pv begins and occurs at the same time of the fixed pulse Pf. The difference area is the error signal. Only one flip flop contributes to the jitter.

B. Both transitions synchronizer - automatic

This synchronizer uses both data transitions and the fixed pulse Pf is produced automatically by the second flip flop (Fig.4).

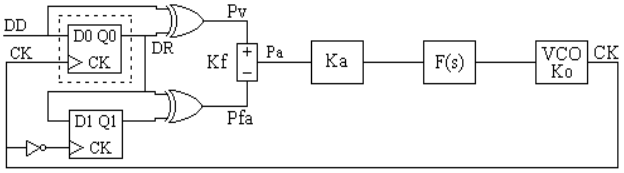

Fig.4 Automatic both transitions synchronizer (seqv-a)

The phase comparator inputs (input and VCO) are both digital. The output is function of the input and state.

Following figure shows the waveforms that illustrate the operation mode of this synchronizer (Fig.5).

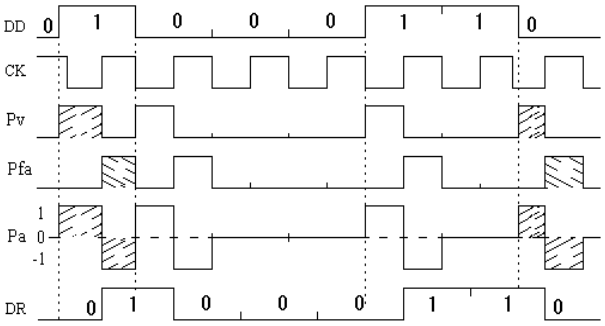

Fig.5 Waveforms of the automatic both transitions (seqv-a)

The variable pulse Pv begins and occurs at different time of the fixed pulse Pf. The difference area is the error signal. Two flip flops contributes to the jitter.

III. POSITIVE TRANSITIONS SYNCHRONIZERS

The synchronizers of positive data transitions uses only the synchronism inf*ormation of the positive data transitions. These synchronizers* make a pulse comparation (variable pulse Pvp and fixe Pfp) only in the positive data transitions [5].

A. Positive transitions synchronizer - manual

This synchronizer uses only the positive data transition and the fixed pulse Pfp is produced with previous manual adjusting of the delay Δt=T/2 (Fig.6).

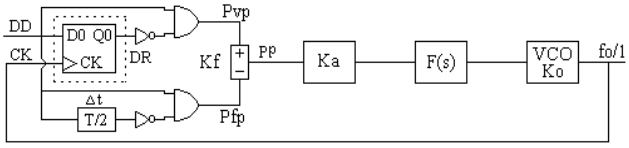

Fig.6 Manual positive transition synchronizer (seqvp-m)

The phase comparator inputs (input and VCO) are both digital. The output is function of the input and state.

Following figure shows the waveforms that illustrate the operation mode of this synchronizer (Fig.7).

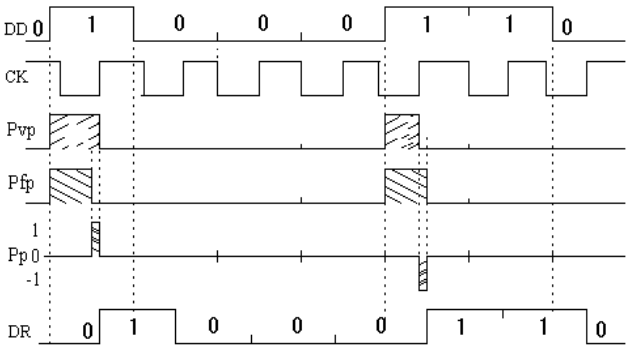

Fig.7 Waveforms of the manual positive transition (seqvp-m)

The variable pulse Pvp begins and occurs at the same time of the fixed pulse Pfp. The difference area is the error signal. Only one flip flop contributes to the jitter.

B. Positive transitions synchronizer - automatic

This synchronizer uses only the positive data transition and the fixed pulse Pf is produced automatically by the second flip flop (Fig.8).

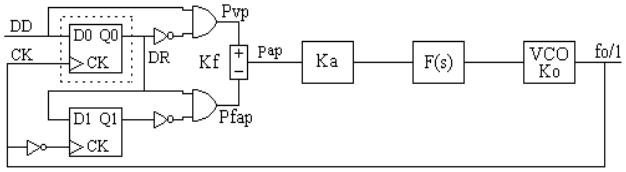

Fig.8 Automatic positive transition synchronizer (seqvp-a)

The phase comparator inputs (input and VCO) are both digital. The output is function of the input and state.

Following waveforms show the operation mode of the automatic sequential digital synchronizer (Fig.9).

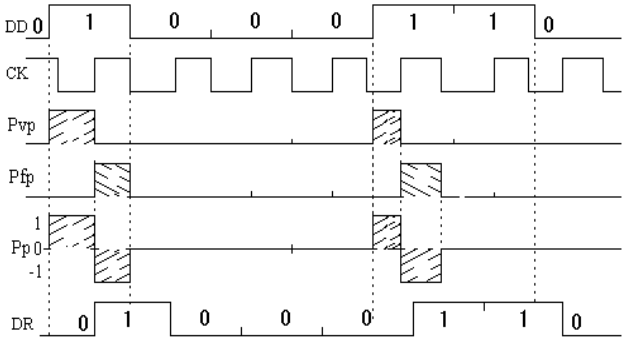

Fig.9 Waveforms of the automatic positive transition (seqvp-a)

The variable pulse Pvp begins and occurs at different time of the fixed pulse Pfp. The difference area is the error signal. Two flip flops contributes to the jitter.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [6].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can unnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = $A^2_{ef}/(No.Bn)$. But, No can be related with the noise variance σn and inverse sampling $\Delta\tau=1/Samp$, then $No=2\sigma n^2.\Delta\tau$, so $SNR=A^2_{ef}/(2\sigma n^2.\Delta\tau.Bn) = 0.5^2/(2\sigma n^2*10^{-3}*5)= 25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s)=\frac{\mathrm{G(s)}}{1+\mathrm{G(s)}}=\frac{KdKoF(s)}{s+KdKoF(s)}=\frac{KdKo}{s+KdKo} \quad (1)$$

the loop noise bandwidth is

$$\mathrm{Bl}=\frac{KdKo}{4}=Ka\frac{KfKo}{4}=0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=1/2; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2/π* (3)

For the hybrid synchronizers, the loop bandwidth is

Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=0.45; Ko=2π)

*(Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2.2/π* (4)

For the combinational synchronizers, the loop bandwidth is

Bl=0.02=(Ka.Kf.Ko)/4 with (Kf=1/π; Ko=2π)

*(Ka*1/π*2π)/4 = 0.02 -> Ka=0.04* (5)

For the sequential synchronizers, the loop bandwidth is

Bl=0.02=(Ka.Kf.Ko)/4 with (Kf=1/2π; Ko=2π)

*(Ka*1/2π*2π)/4 =0.02 -> Ka=0.08* (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl. For the analog PLL the jitter is

$\sigma\phi^2 = Bl.No/Aef^2 = \mathrm{Bl}.2.\sigma n^2.\Delta\tau/Aef^2 = 0.02*2\sigma n^2*10^{-3}/0.5^2 = 16*10^{-5}.\sigma n^2$

For the others PLLs the jitter formula is more complicated.

- 2nd order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

Fig.10 shows the setup that was used to test the various synchronizers.

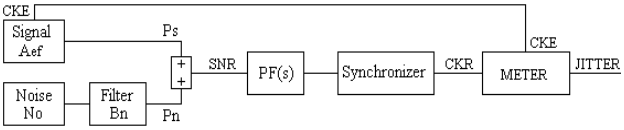

Fig.10 Block diagram of the test setup

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

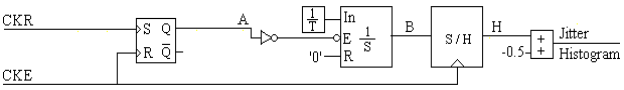

Fig.11 The jitter measurer (Meter)

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (output jitter UIRMS - input SNR) for the four sequential symbol synchronizers.

Fig.12 shows the jitter-SNR curves of the synchronizers: both transitions - manual (seqv-m), both transitions - automatic (seqv-a), positive transition - manual (seqvp-m) and positive transition - automatic (seqvp-a).

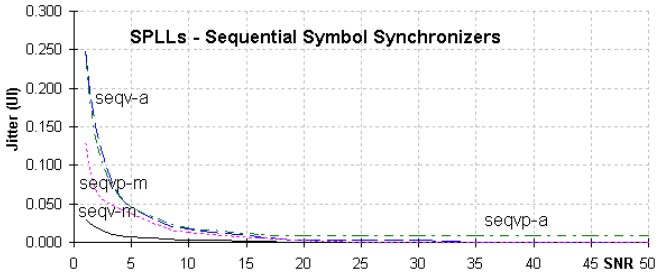

Fig.12 Jitter-SNR curves of the four synchronizers(b-m,b-a, p-m,p-a)

We verify, that generally the output jitter UIRMS diminishes exponentially with the input SNR increasing.

For high SNR, the four curves tend to be similar although with a small disadvantage of the positive transition - automatic (seqvp-a). However, for low SNR the both transitions - manual (seqv-m) is the best, followed of the positive transition -manual (seqvp-m) and the both transitions - automatic (seqv-a) and the positive transition - automatic (seqvp-a) are the worst and similar.

V. CONCLUSIONS

We studied four sequential symbol synchronizers, namely the both transitions - manual (seqv-m), both transitions - automatic (seqv-a), positive transition - manual (seqvp-m) and positive transition - automatic (seqvp-a).

We tested their output jitter UIRMS versus input SNR.

We observed that, generally, the jitter diminishes almost exponentially with the SNR increasing.

We verified, that for high SNR, the jitter of the four synchronizers are similar, although with a litle disadvantage of the positive transition - automatic (seqvp-a), this is comprehensible since it has two flip flops and stays more time in the error state until the next correction transition.

However, for low SNR, the both transitions - manual (seqv-m) is the best since only one flip flop contributes to the error state and the time in the error state is lesser. After is the positive transition - manual (seqvp-m) since only one flip flop contributes to the jitter but the time in the error state is greater (two times). At last are the two automatic versions (seqv-a, seqvp-a) since they have two flip flops that contributes to the jitter and are similar. Anyway, the last is still aggravated by the more time in the error state.

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