cognitive radio (plug 2010 award)

nuno carvalho[1], josé vieira[2], arnaldo oliveira[1], pedro cruz[1], daniel albuquerque[2], nelson silva[1]

[1] department of electronics, telecommunications and informatics & instituto de telecomunicações (IT), university of aveiro.
[2] department of electronics, telecommunications and informatics & institute of electronics and telematics engineering of aveiro (IEETA), university of aveiro

Nowadays, new telecommunications standards or new releases of existing ones (e.g., Worldwide Interoperability for Microwave Access (WiMAX), 3GPP Long Term Evolution (LTE), Universal Mobile Telecommunications System (UMTS), High Speed Downlink Packet Access (HSDPA), etc) are constantly appearing. In this scenario, interoperability across existing standards is a crucial requirement to achieve a high quality of service (QoS). Software Defined Radio (SDR) technology holds the best promise of meeting this requirement whilst efficiently tackling the ever-increasing complexity of radio systems.

One of the most interesting potential applications of SDR is to increase the spectrum occupancy by designing opportunistic radio systems, i.e. systems capable of dynamically allocating regions of the spectrum that happen to be free at a given moment, which implies the ability to "see" or "be aware" of the entire spectrum and its usage at a precise time. This has motivated the scientific community to study different radio architectures with the ability of detecting signals over a broad frequency band with a high dynamic range. This requirement poses problems due not only to bandwidth restrictions but also to high peak-to-average power ratio (PAPR) demands or RF interference from one or more sources.

Building flexible multi-mode/multi-standard SDR and Cognitive Radios (CR) requires digital processing of high-frequency and wide-band signals, which is challenging in terms of sampling rate, operating speed, dynamic range and power consumption. For this reason, a purely software-based implementation using off-the-shelf Digital Signal Processor (DSP) units is hardly feasible. It is necessary to resort to specialized hardware devices, e.g. based on Field Programmable Gate Arrays (FPGAs). The large integration capacity and advanced features of modern FPGAs make them appealing for an increasing number of practical applications. Their reconfigurability makes them particularly suited for applications requiring fast design cycles, dynamic adaptation and/or field updates.